

# MS-7638 Ver: 1.0

## CPU:

INTEL - Lynnfield/ Clarkdale LGA 1156

## System Chipset:

INTEL-IBEXPEAK PCH (H - 57)

## OnBoard Chipset:

Clock Gen:ICS 4105B

IDE X1 JMB-368

HD Audio Codec:ALC889

LAN:RTL8111D 10/100/1000

SIO:F71889

Flash ROM: 64 Mb SPI (CHIP)

## Main Memory:

DDRIII (800/1066/1333MHz) \* 4 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 2

PCI Express (X1) Slot \* 2

PCI Slot \*3

## PWM:

Controller: uP6206

( 3-Phase use STD MOS -- 95W )

OV by uP6264 or SIO

uP6103 (CPU\_VTT)

Linear (PCH)

uP6103(DDR)

GPU Power -ISL6314

## ACPI: uPI+SIO

## Other:

SATA(SATA2-300MB/s) \*6

USB2.0 \*10 (Rear\*4 / Front\*6)

PRINT Header \*1

COM pin header \*2

TPM Header \*1

on BOARD BUZZER

D-SUB \*1

DVI PORT\*1

HDMI PORT\*1

## BOM SKUs

H55:chiset

S:solid cap

EL:EL cap

G:giga lan 8111DL

M:Miga lan 8103EL

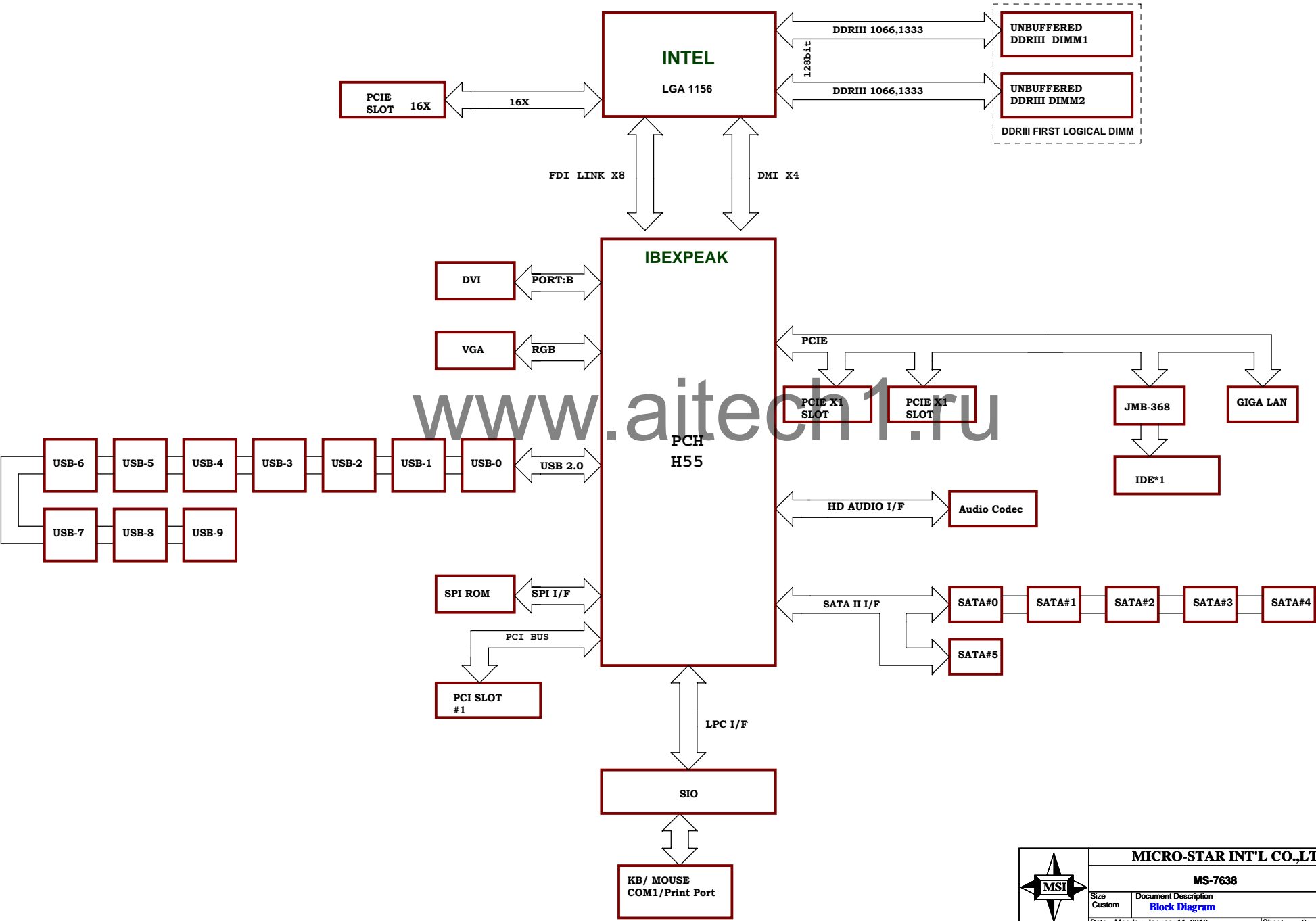
6: 6 ports

DVI: DVI Stuff

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## DDR DIMM config.

Device	Address	Clock
CHA DIMM1	10100001B	MEM_MA_CLK_H0/L0 H1/L1
CHB DIMM2	10100000B	MEM_MB_CLK_H0/L0 H1/L1

## PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#A PCI_INT#B PCI_INT#C PCI_INT#D	PCI_REQ0# PCI_GNT0#	AD16	PCH CLKOUT_PCI<0>
TPM				PCH CLKOUT_PCI<3>
SIO				PCH CLKOUT_PCI<2>

TABLE 9↓  
USB PORT MAPPING (SUBJECT TO CHANGE)

Controller	Port	Destination	Fused	ESD Pads	Bulk Cap	Over-Current Detection
UHCI #1, EHCI #1	Port 0	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
	Port 1	Internal (Ready Boost - P151)	Yes	Yes	No	Yes
UHCI #2, EHCI #1	Port 2	Internal (Media Reader - P150)	Yes	Yes	No	Yes
	Port 3	Internal (Media Reader - P150)	Yes	Yes	No	Yes
UHCI #3, EHCI #1	Port 4	Front I/O	Yes	Yes	No	Yes
	Port 5	Front I/O	Yes	Yes	No	Yes
UHCI #4, EHCI #2	Port 6	Front I/O	Yes	Yes	Yes	Yes
	Port 7	Front I/O	Yes	Yes	Yes	Yes
UHCI #5, EHCI #2	Port 8	Rear I/O	Yes	Yes	Yes	Yes
	Port 9	Rear I/O	Yes	Yes	Yes	Yes
UHCI #6, EHCI #2	Port 10	Rear I/O	Yes	Yes	Yes	Yes
	Port 11	Rear I/O	Yes	Yes	Yes	Yes
UHCI #7, EHCI #2	Port 12	Rear I/O	Yes	Yes	Yes	Yes
	Port 13	Rear I/O	Yes	Yes	Yes	Yes

## PCI RESET DEVICE

IBEXPEAK	
Signals	Target
PCIRST#_PCH	PCISLOT1
PLTRST_BU1#	JMB368 IDE
PLTRST_BU2#	PCIE*16 / *1
PLTRST_BU3#	LAN&TPM
PLTRST#	SIO



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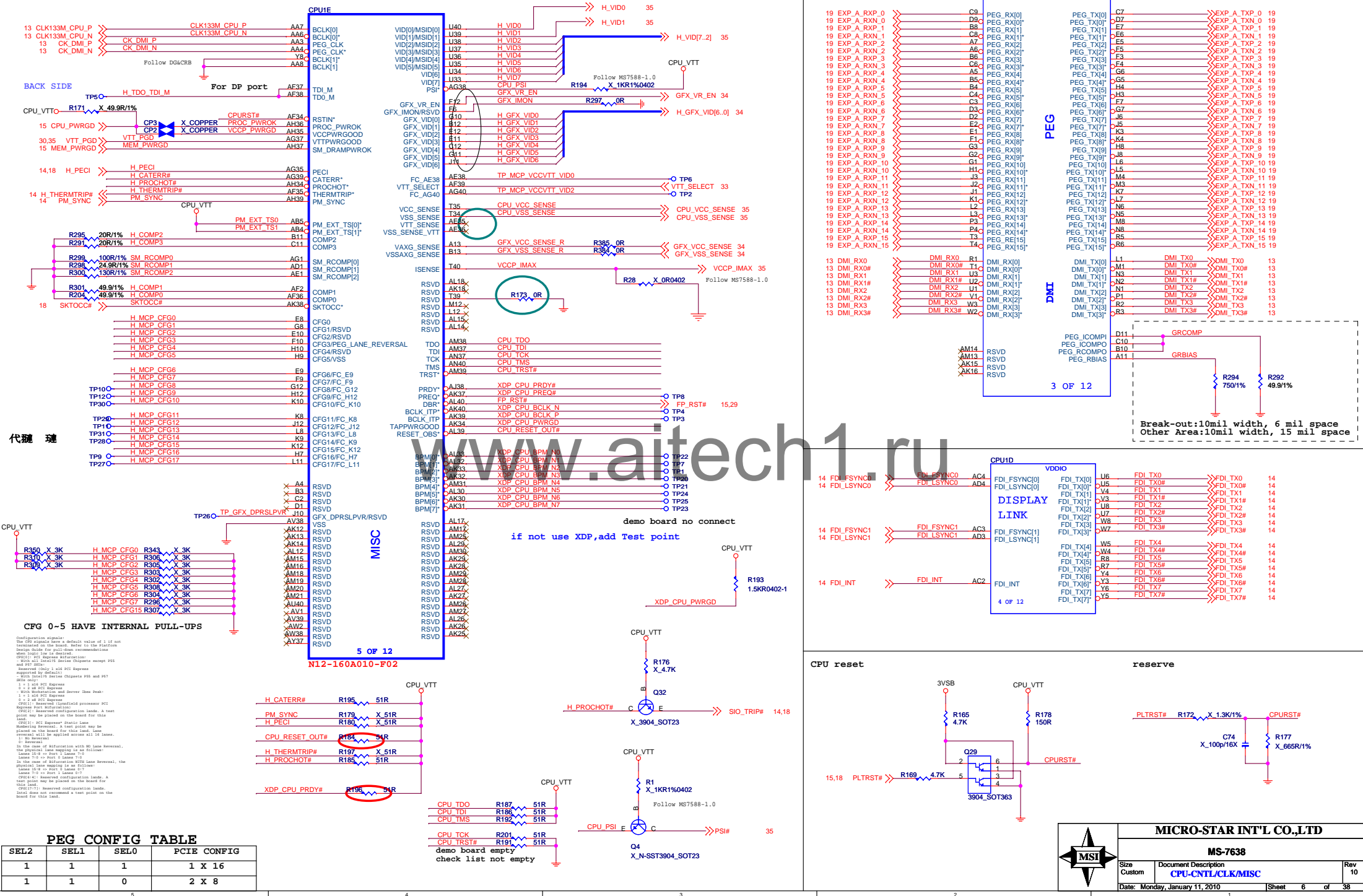
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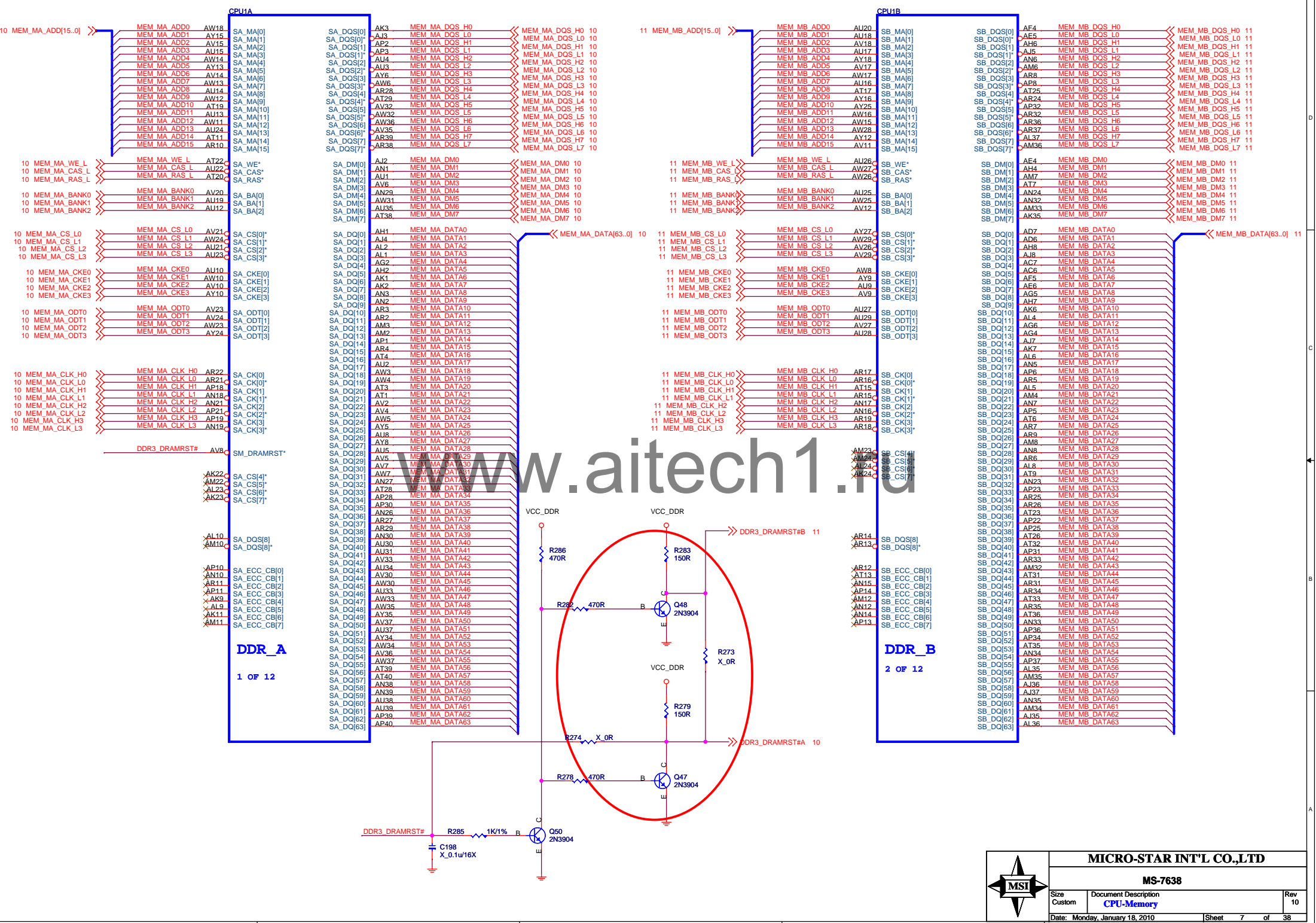
- 1.2009-10-13 Change VCC\_SENSE to CPU\_VCC\_SENSE
- 2.2009-10-13 Add HDMI circuit,change USB circuit,JSP1 circuit update
- 3.2009-10-13 update NCT3016 circuit ,add VTIN3 circuit for VRM MOS
- 4.2009-10-18 Add C589 C590
- 5.2009-10-18 Add R561 R562 For HDMI HPDET
- 6.2009-10-20 Add R602,Swap HDMI wire for layout
- 7.2009-10-21 NCT3016 circuit update:add R637 Q65 R592,Change U27 pin16 tp NCT\_GPIO16,delete C121
- 8.2009-10-21A NCT3016 citcui update:add Q85,chang SATA1&SATA2 to SATA1\_2
- 9.2009-10-23 change JUSB2 & JUSB1 for layout
- 10.2009-10-23A NCT3016 circuit update:add R850
- 11.2009-10-24 delete VCCGATE and DUALGATE circuit
- 12.2009-10-26 delete C534
- 13.2009-10-26 Swap RN40

change to MS-7638-0A

1. 2009-11-09 添加1394---VIA 6315N
2. 2009-11-09 EUP-改用F71889ED
3. 2009-11-09 Page23 添加SATA3.0-23 MARVELL
4. 2009-11-09 Page36 去除debug port 预留
5. 2009-11-09 添加PCIE 4X slot
6. 2009-11-09 添加两个PCI slot
7. 2010-01-04 Power solution:  
R7=21K(R11-0213T13-W08)  
R110=34k(R11-0343T13-W08)  
R18=R51=R71=51.1K(R11-5112T12-W08, ocp=108a)  
R48=13K (R11-0133T23-W08, thermal balance)  
R364=43.2K(R11-4322T12-W08, GPU\_CORE Droop)
8. 2010-01-11 C601改top層, 並上件  
Add HDA co-lay PCIEx1,add R840 R841 RN40  
Remove BUZ1
9. 2010-01-11 JPW1&JBAT1的料號請更換成N41-1030141-H06
- 10.2010-01-11 R693上件
- 11.2010-01-13 Remove C179 for SI VGA
- 12.2010-01-13 R208 change to 330ohm for SI HDMI
- 13.2010-01-13 預留R842位置
- 14.2010-01-18 L3/L4/L5上件120nH, C157/C165/C169上件20p for EMI
- 15.2010-01-18 C337上件0.1u, C102/ C99/ C148/ C186上件0.1u, C412/C414/C419上件10p for EMI
- 16.2010-01-18 stuff R189,Q30 ,Remove D4 for SI
- 17.2010-01-18 stuff R536 R684 R690 Q74 Q76 Q82 Q83 for F71889ED LAA
- 18.2010-01-18 Remove R530 R545 R650 R683 R688 for F71889ED LAA
- 19.2010-01-18 ADD R844 C605,change R276(10K) R697(10R)for F71889ED LAA
- 19.2010-01-18 ADD R88 R247,Remove R91 R246 R810 R818 for F71889ED LAA

AAB8/Y8 ,these signals for 120 MHz from the Intel CPU\_P /CLKOUT\_BCLK1\_P and CLKOUT\_DP\_N / CLKOUT\_BCLK1\_N. Leave as NC on the PCH and connect directly to GND at the processor. 120MHz clock is used for embedded DisplayPort which is no supported on Desktop designs.

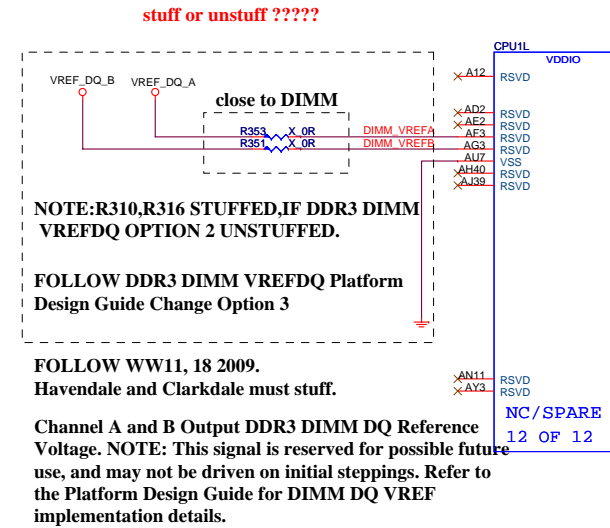
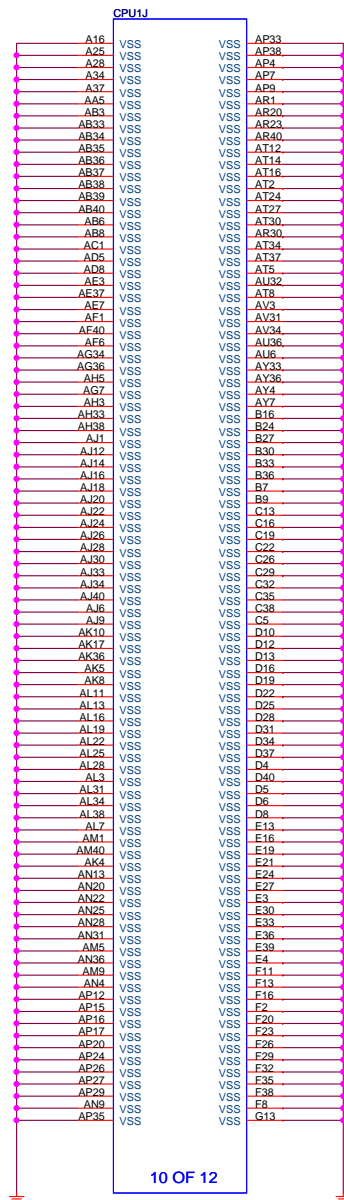






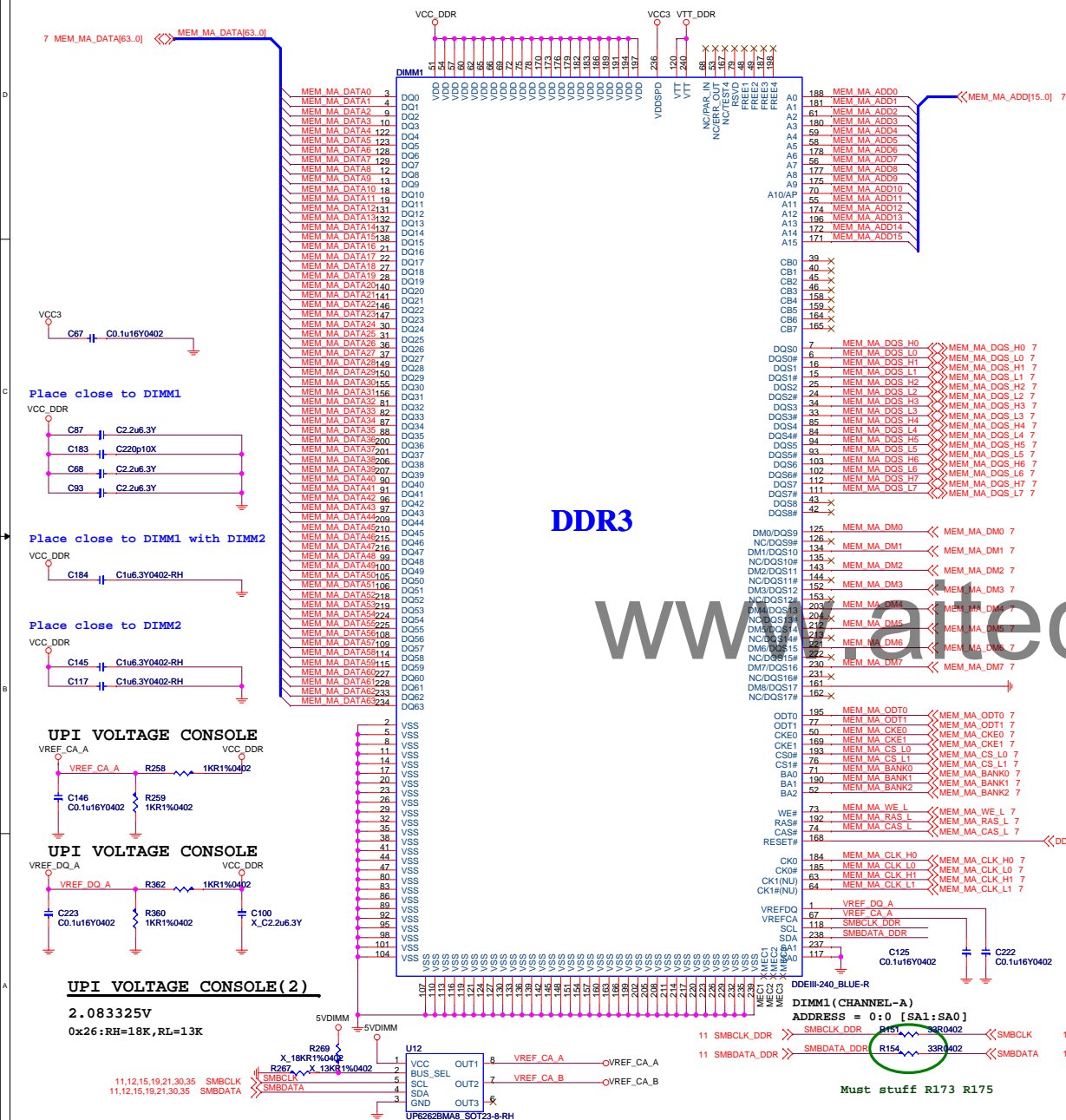




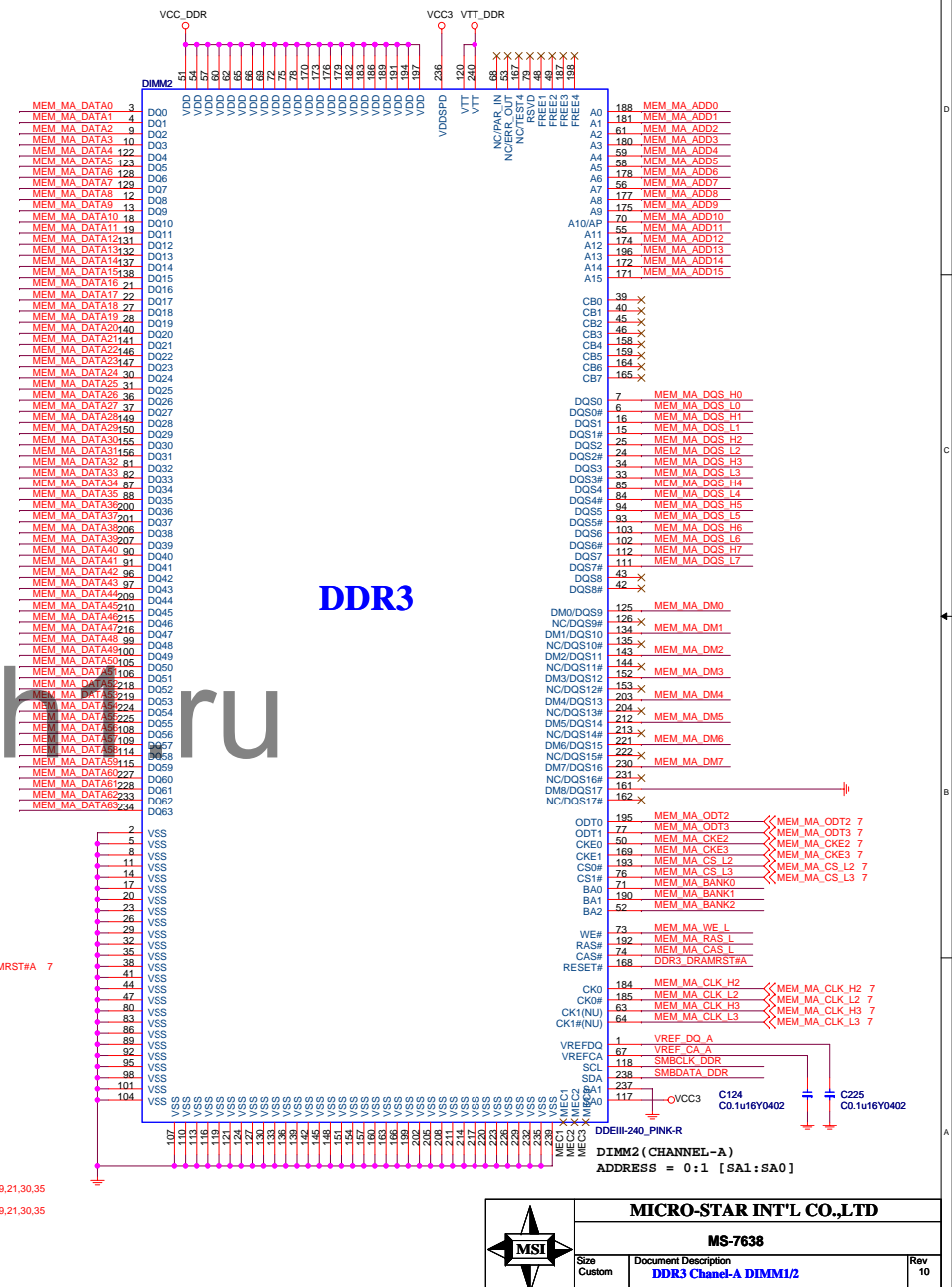


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## DDRIII DIMM\_A1



## DDRIII DIMM\_A2



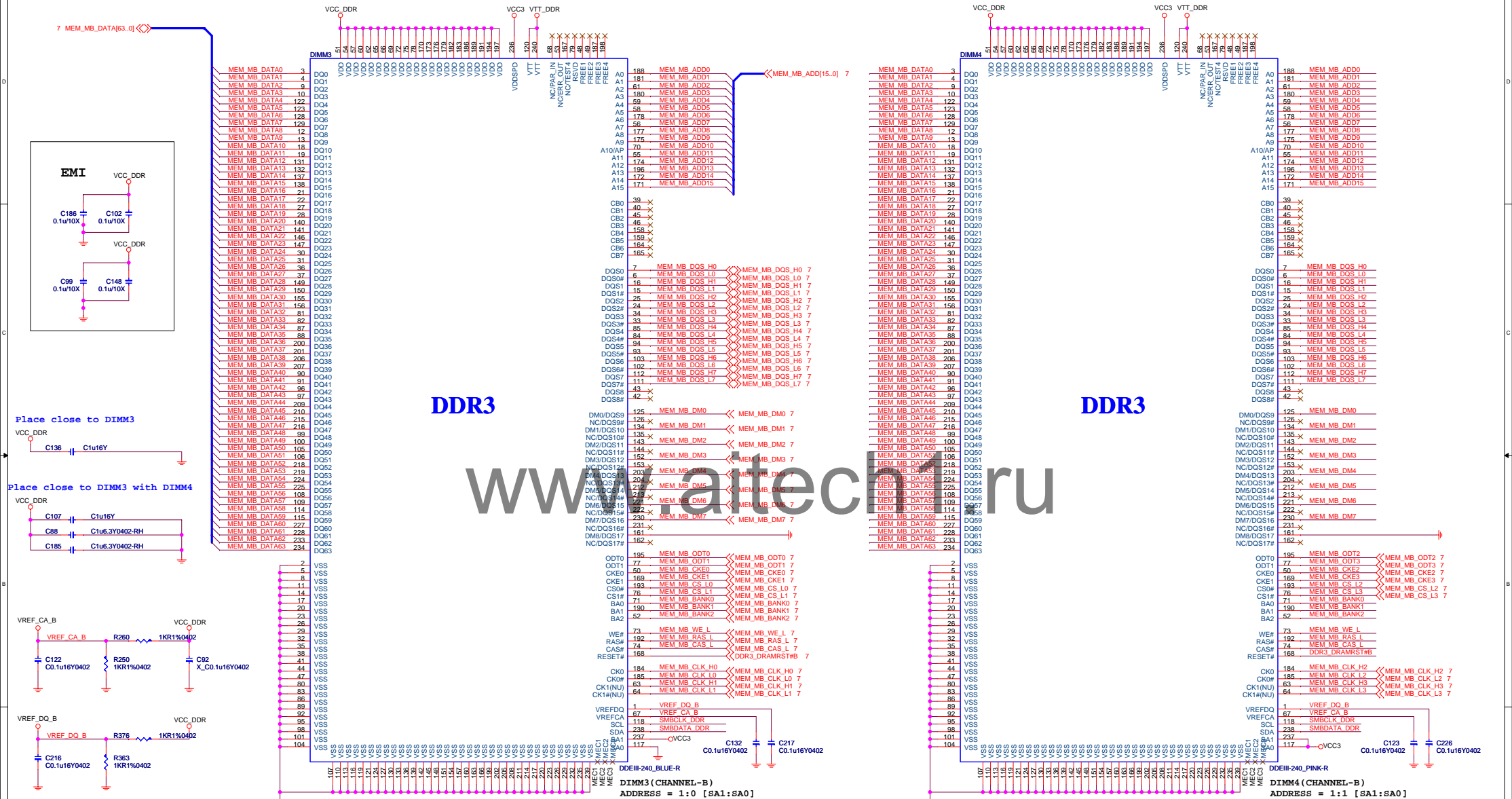
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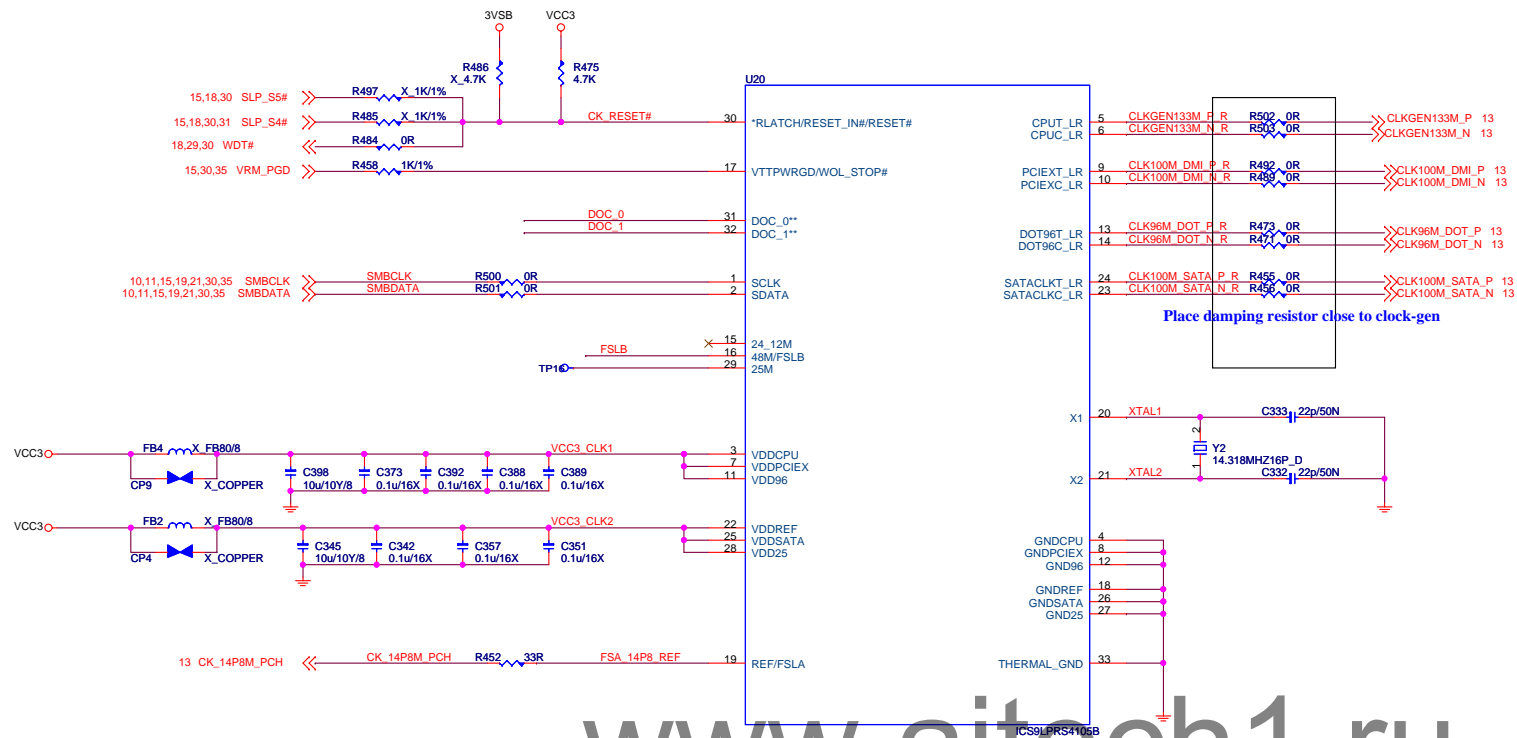
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# DDR3 DIMM\_B1

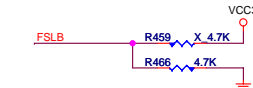
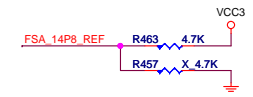
# DDR3 DIMM\_B2





## CLOCK GEN STRAPING

FS4	FS3	FS2	FSB	FSA	CPU	Spread
B0b4	B0b3	B0b2	B0b1	B0b0	Mhz	%
0	0	0	0	0	100.00	-0.5
0	0	0	0	1	133.33	-0.5
0	0	0	1	0	200.00	-0.5
0	0	0	1	1	166.66	-0.5

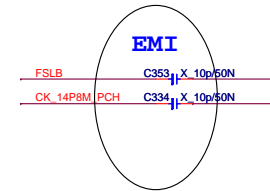
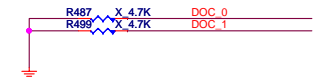


Pin16: 48MHz clock output. / 3.3V tolerant input for CPU frequency selection. Low voltage threshold inputs, see input electrical characteristics for Vil\_FS and Vih\_FS values.

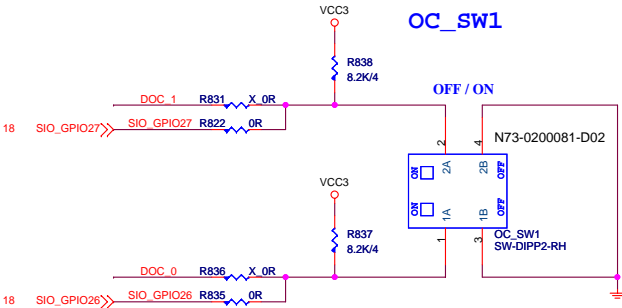
Pin19: 14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil\_FS and Vih\_FS values.

## OC

DOC\_0\*:Dynamic Over Clocking pin: real time frequency selection 0: Normal; 1: Frequency will transition to a preprogrammed value in the I2C.



## OC\_SW1



OFF=1 ; ON=0

DOC	TABLE
1 0	CPU FREQUENCY
1 1	133 MHz ( default )
1 0	142 MHz
0 1	150 MHz
0 0	166 MHz

( Default ) OFF / OFF

OFF / ON

ON / OFF

ON / ON

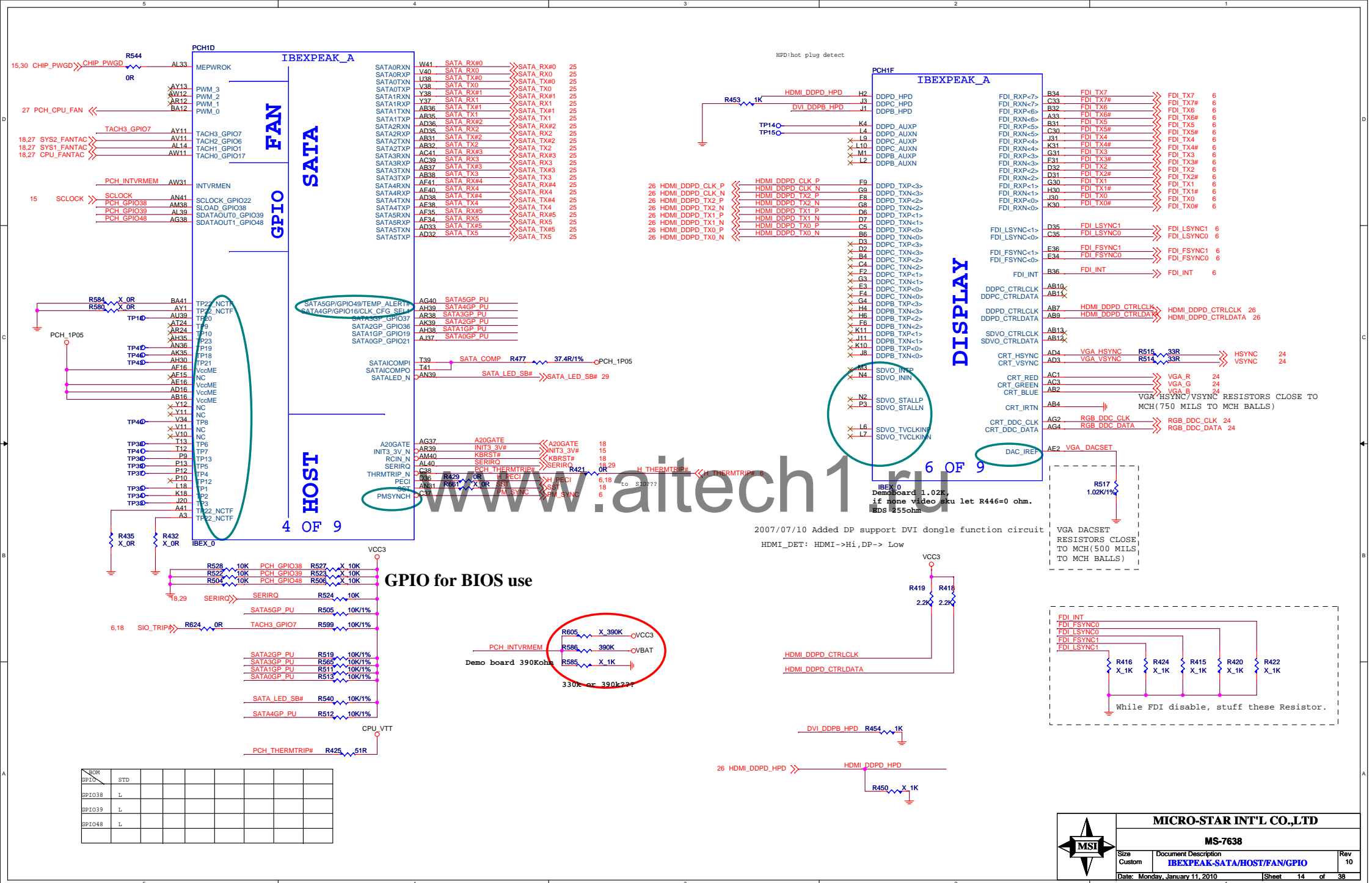


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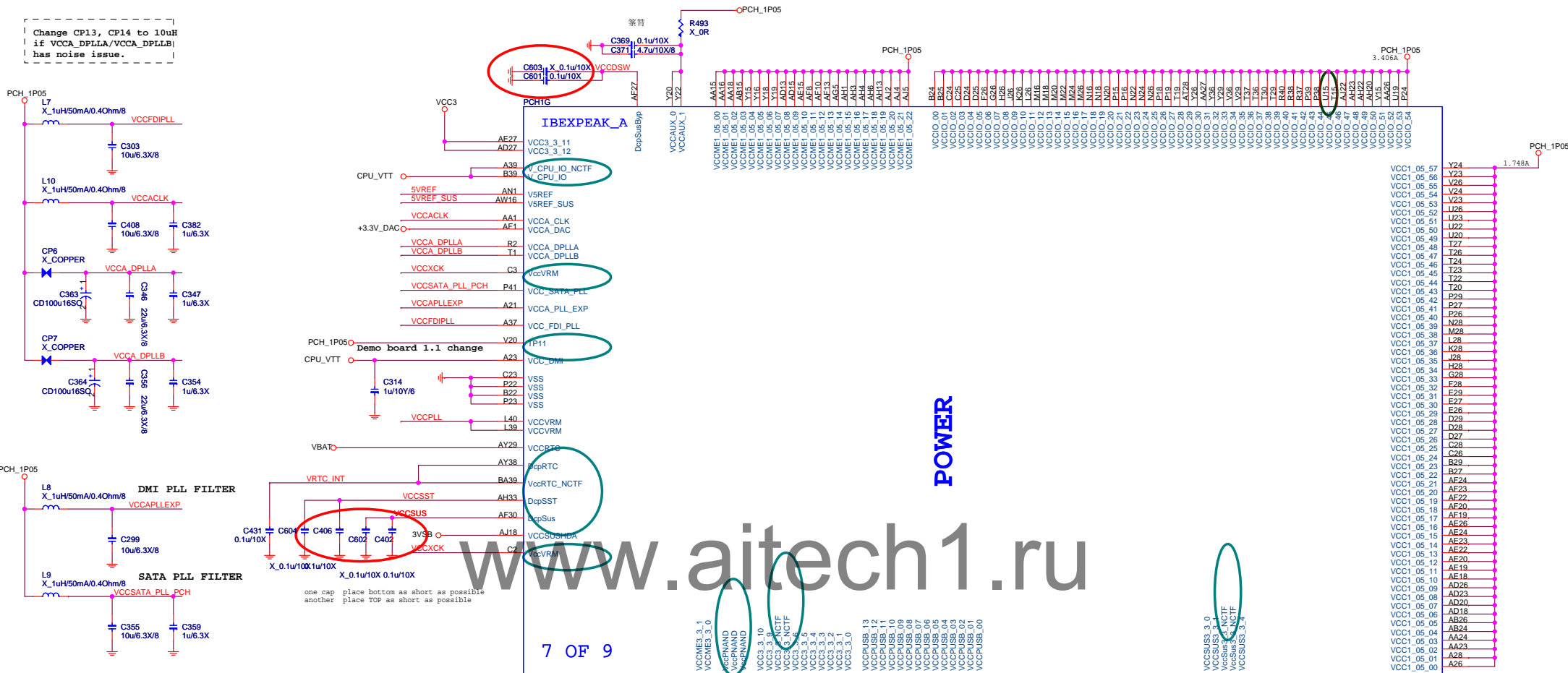






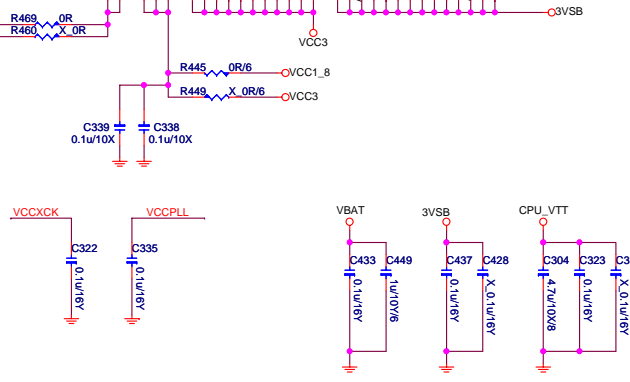
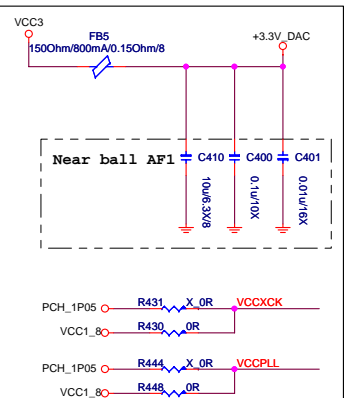
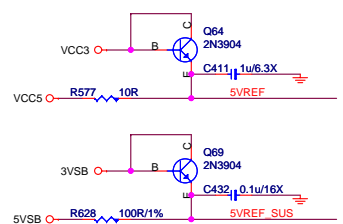




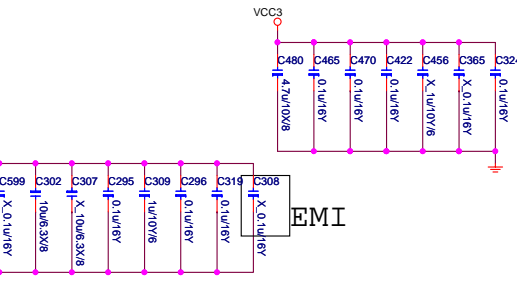


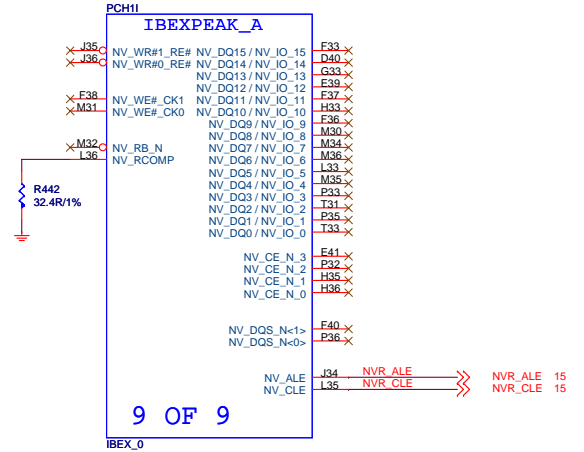
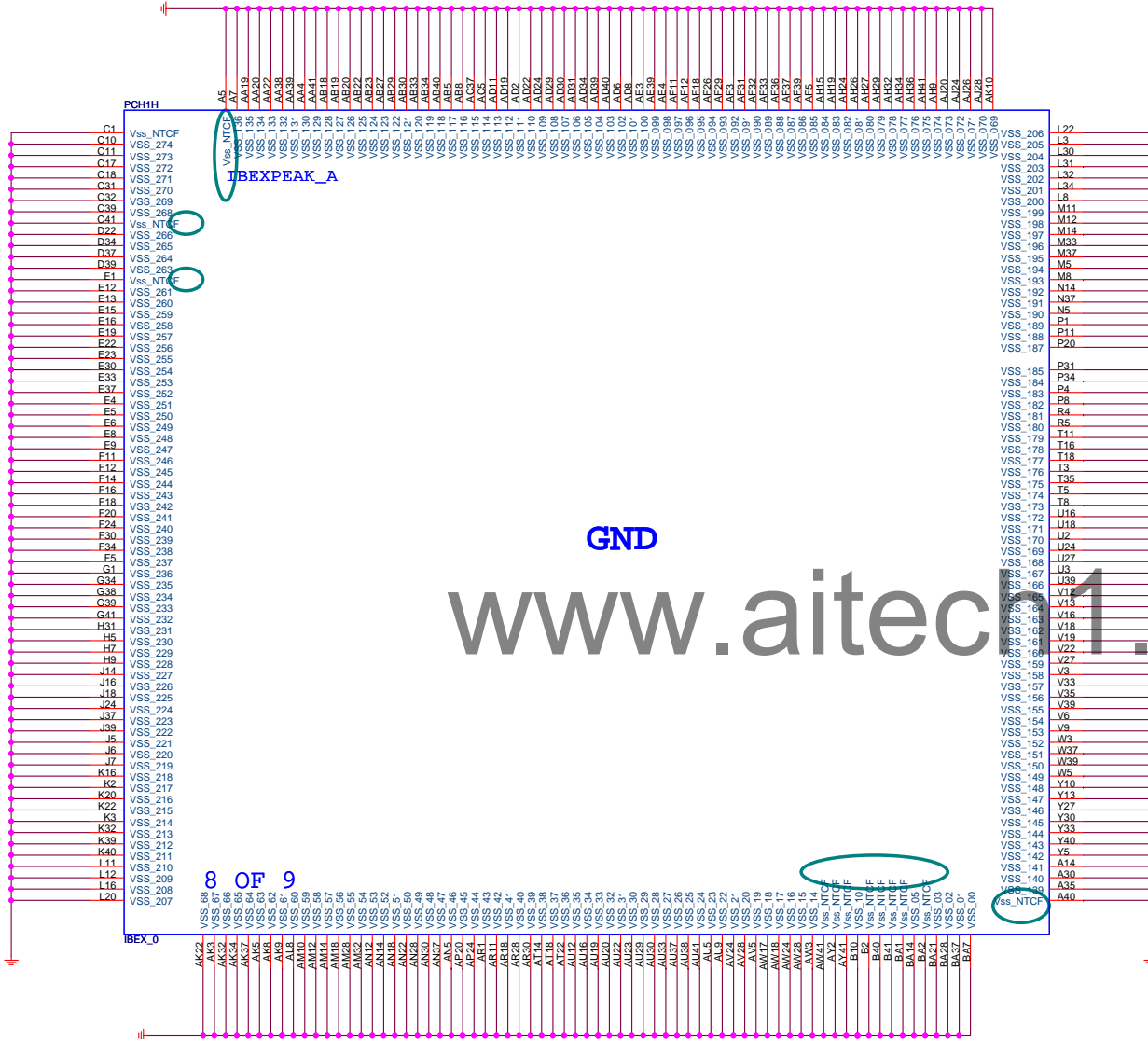
### 5VREF & 5VREF\_SUS Sequencing Circuit

V5REF must be powered up before VCC3 or after VCC3 within 0.7V. Also, V5REF must power down after VCC3 or before VCC3 within 0.7V. This rule is also applies to V5REF\_SUS and 3VSB. However, the 3VSB is derived from the 5VSB on the power supply thru a voltage regulator and therefore, they can satisfy the requirement.



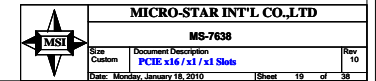
## PCH decoupling cap



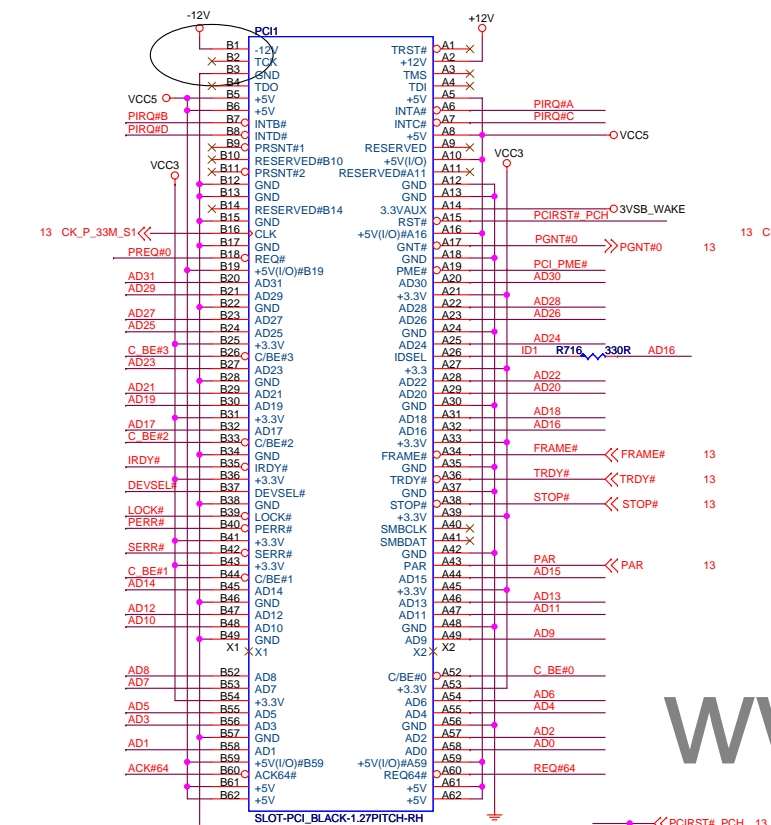




**PCI EXPRESS x1-PORT2**

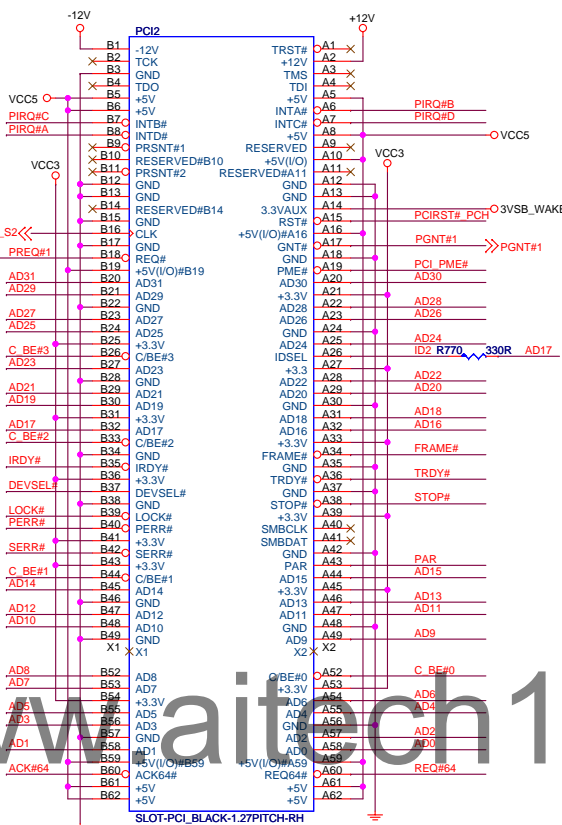


# PCI SLOT 1 (PCI VER: 2.2 COMPLY)



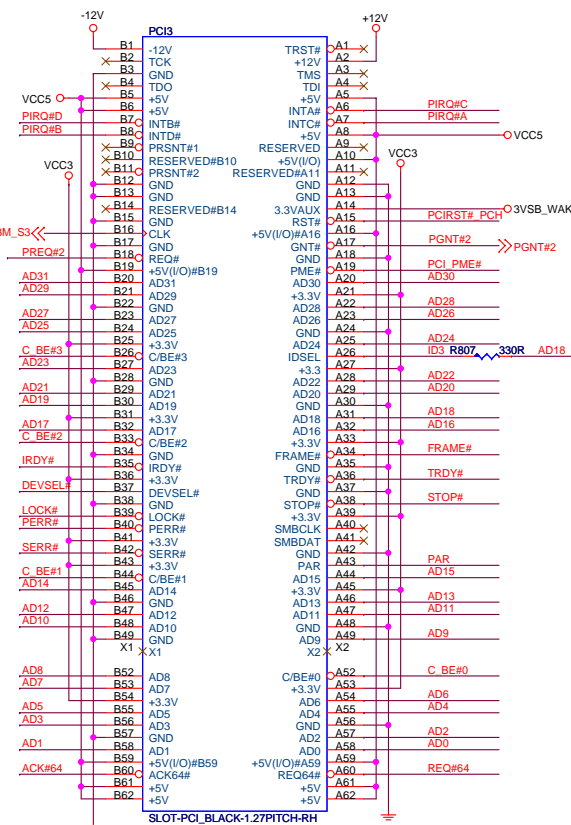
ISDEL = AD16  
MASTER = PREQ#0  
PIRQ#A

# PCI SLOT 2 (PCI VER: 2.2 COMPLY)



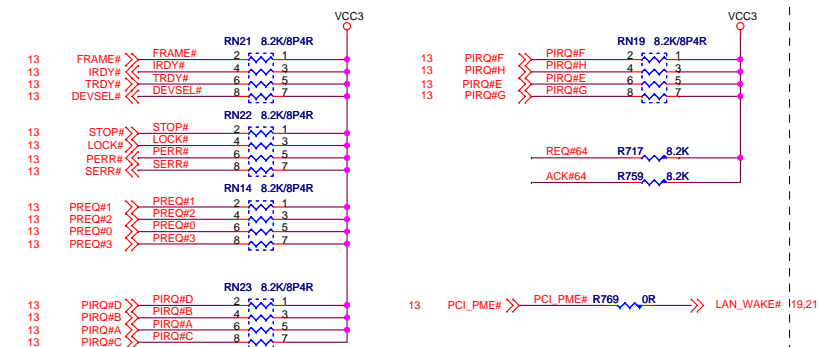
ISDEL = AD17  
MASTER = PREQ#1  
PIRQ#B

# PCI SLOT 3 (PCI VER: 2.2 COMPLY)

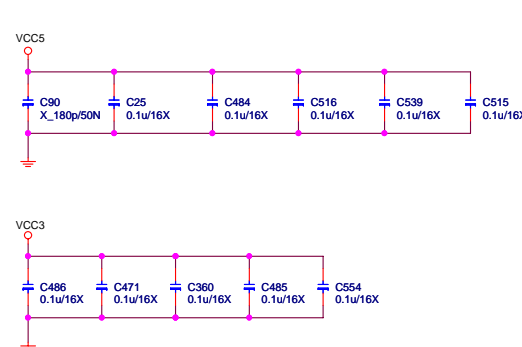


ISDEL = AD18  
MASTER = PREQ#2  
PIRQ#C

## PCI PULL-UP / DOWN RESISTORS



## PCI SLOT DECOUPLING CAPACITORS



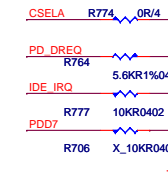
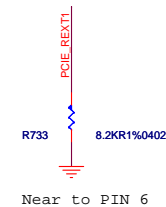
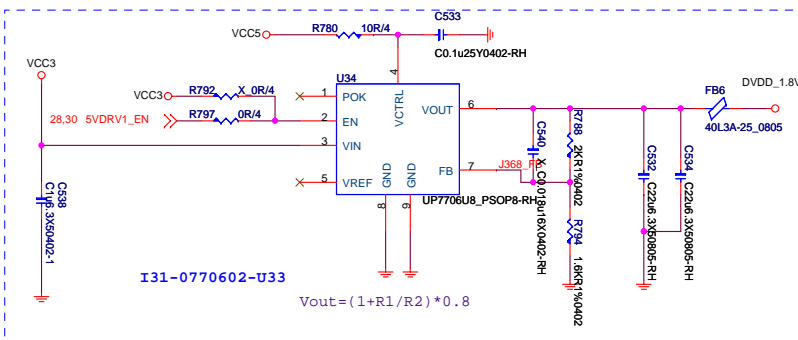
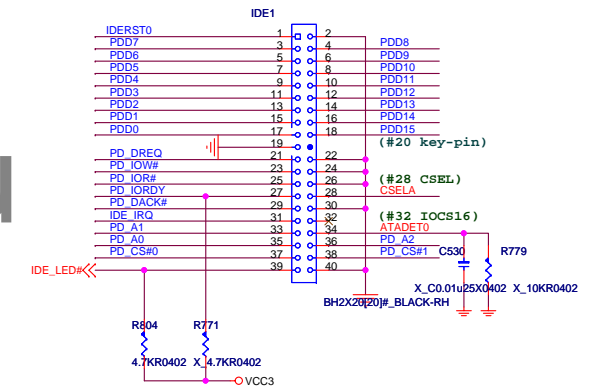
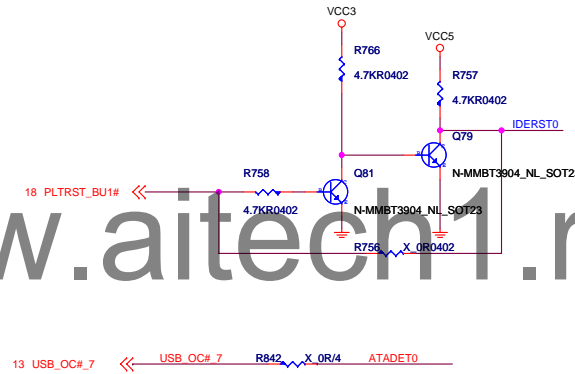
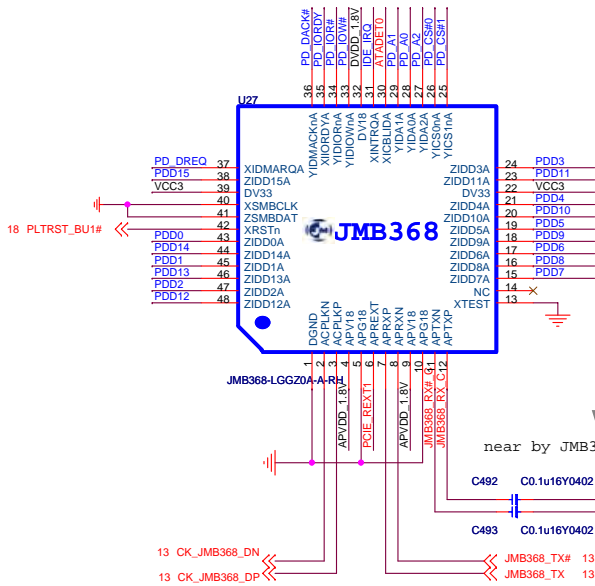
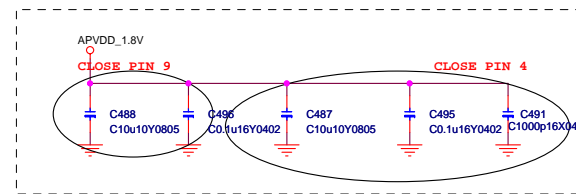
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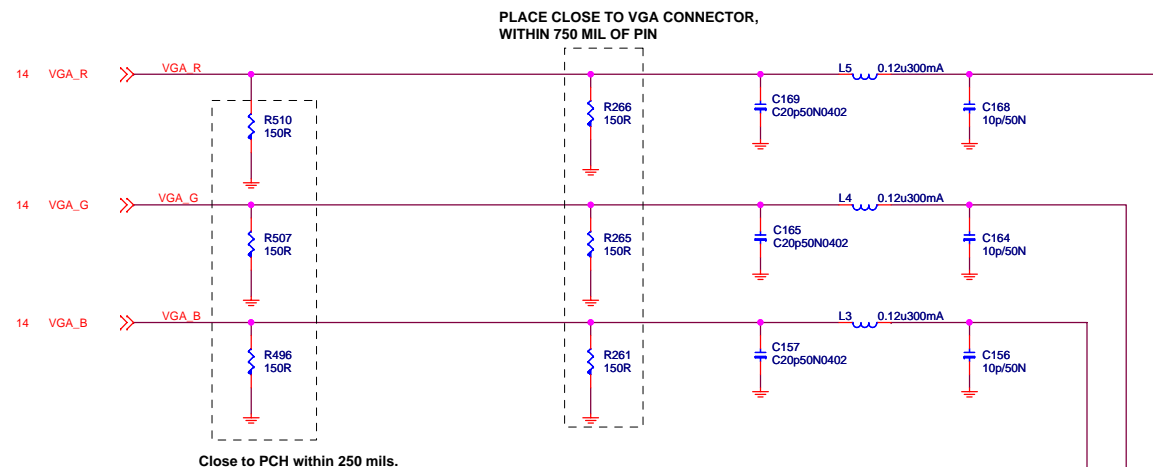
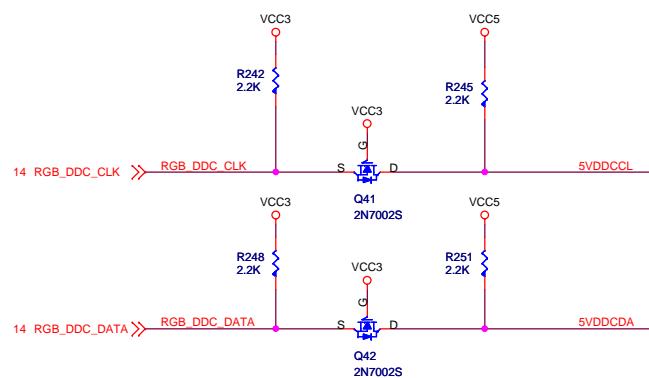




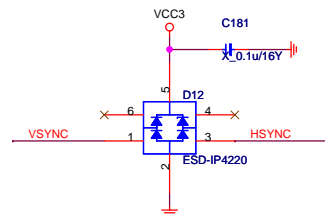
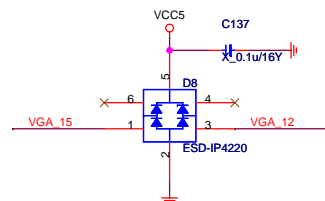
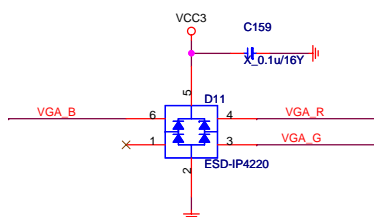
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# D-Sub

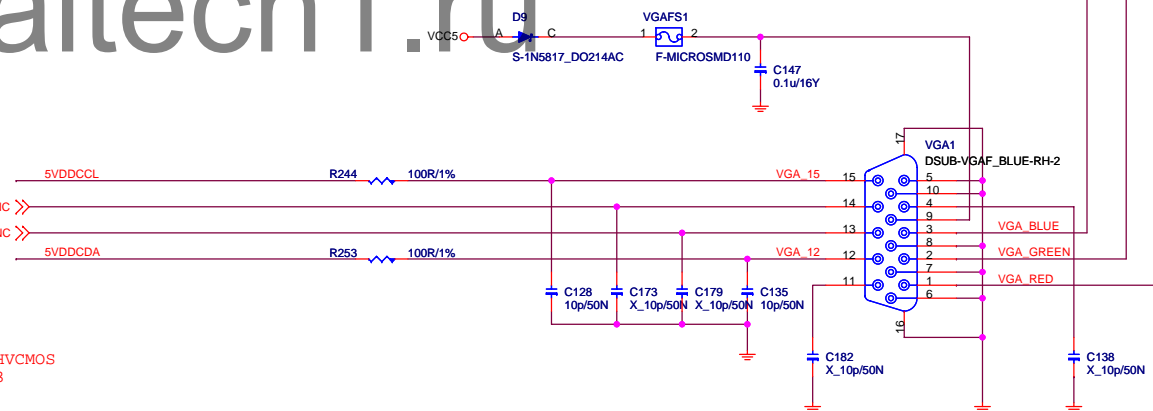
## Level shift



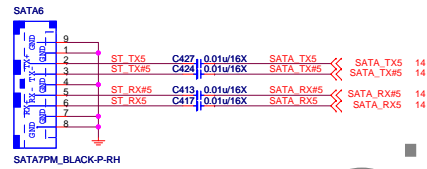
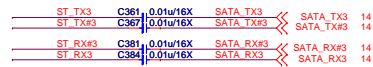
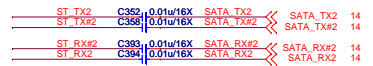
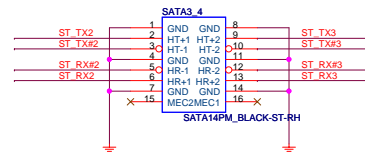
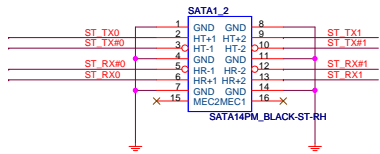
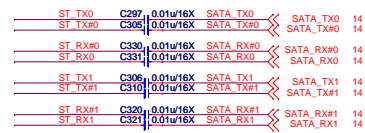
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VSYNC/HSYNC:HVCMS  
CRB pull VCC3

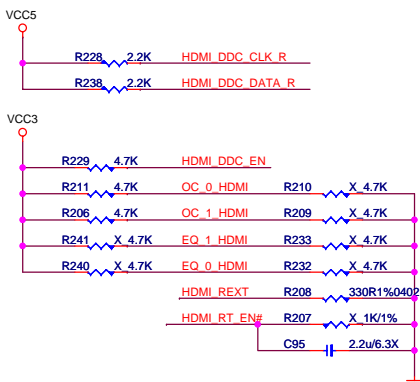
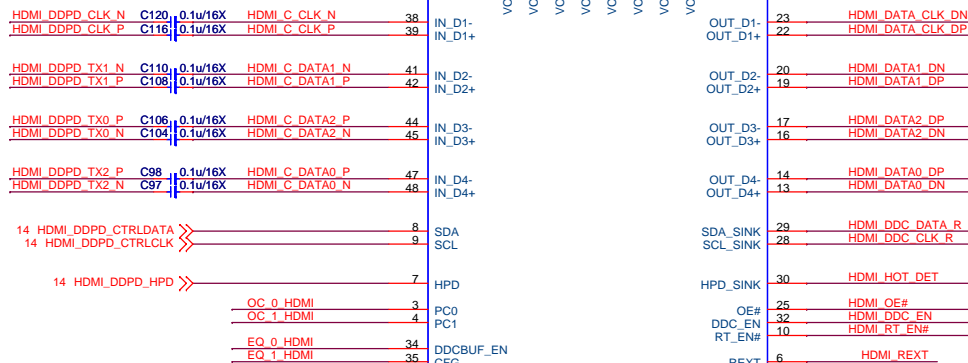


# SATA connector (color:Black)



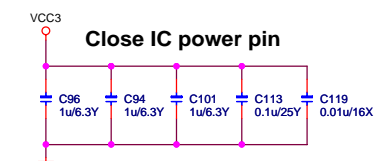
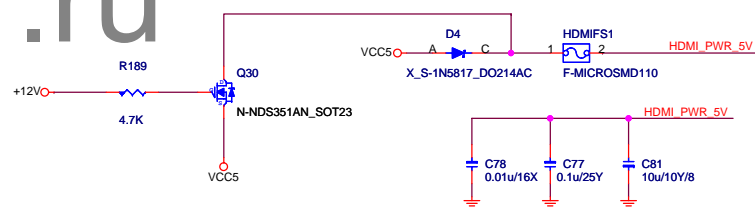
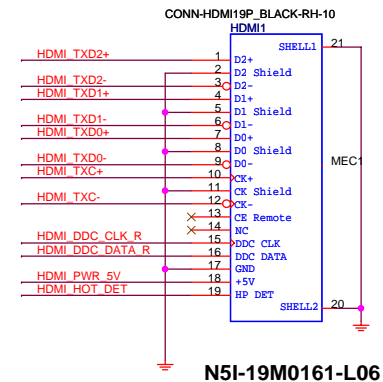
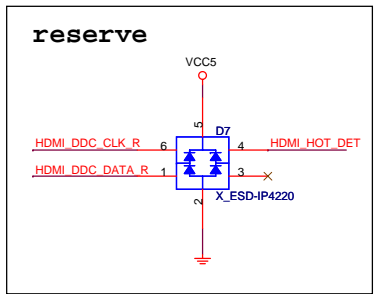
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# HDMI level shifter



PERICOM 腹:BOB-411LS2C-P22.  
PARADE 腹:BOB-081010C-P97.

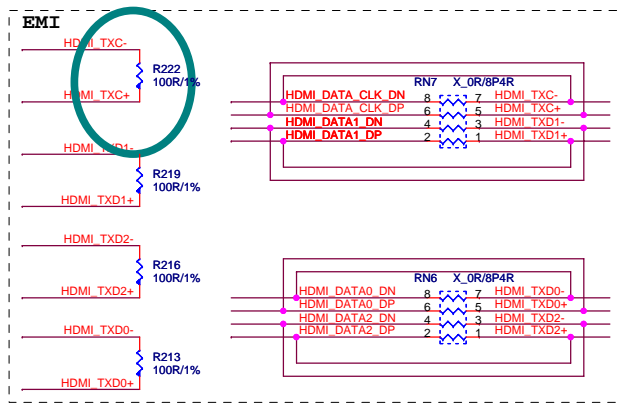
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	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

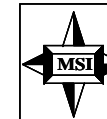
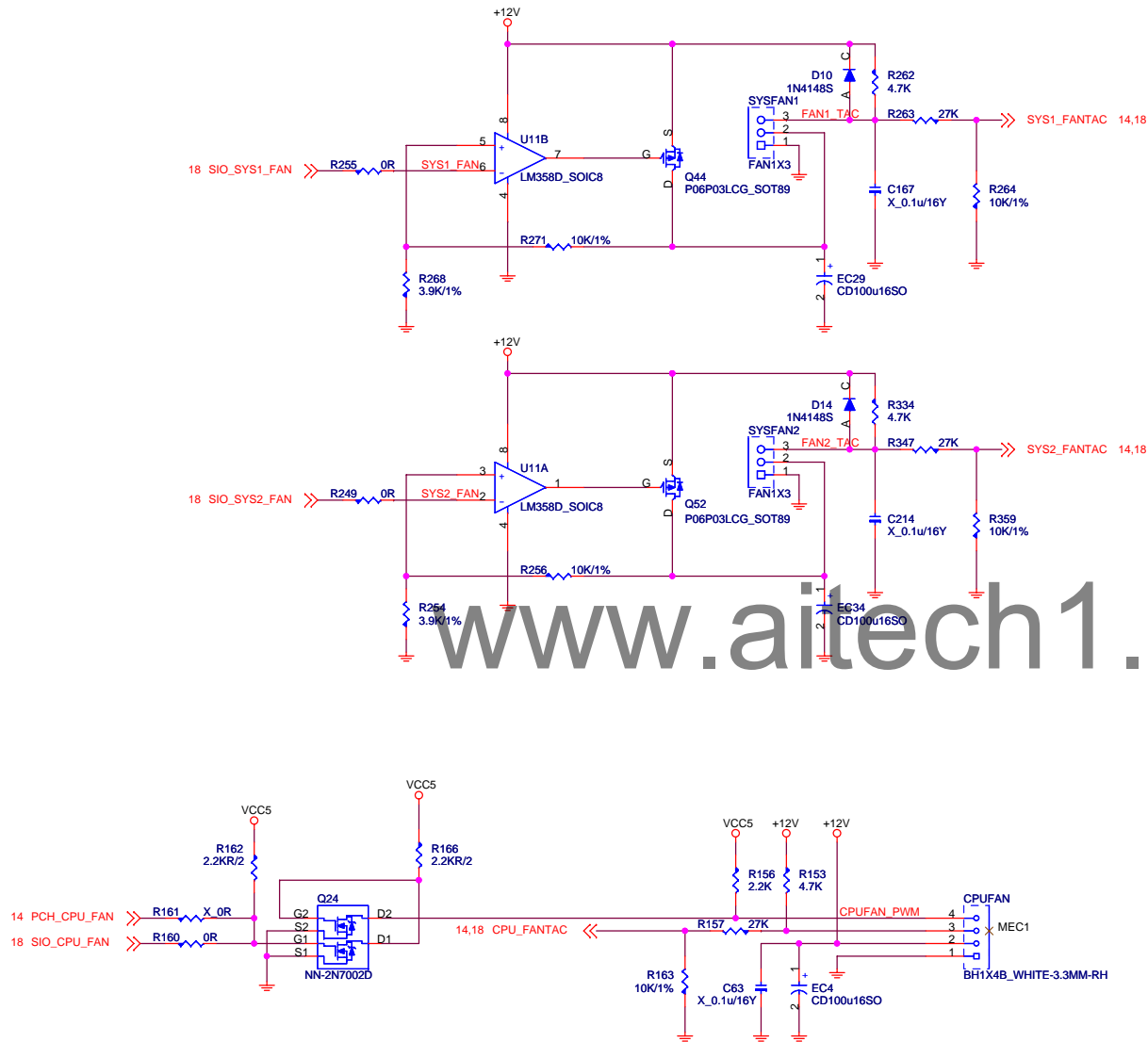
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	



**MICRO-STAR INT'L CO.,LTD**  
**MS-7638**  
Size Custom | Document Description **HDMI** | Rev 10  
Date: Thursday, January 21, 2010 | Sheet 26 of 38

# FAN-COUNTROL CIRCUIT



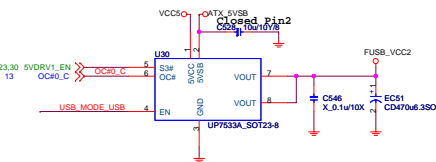
MICRO-STAR INT'L CO.,LTD

MS-7638

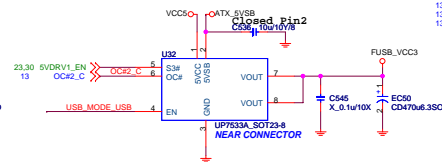
Size	Document Description	Rev
Custom	Fan Control	10
Date: Monday, January 11, 2010	Sheet 27 of 38	

## Rear USB Connector

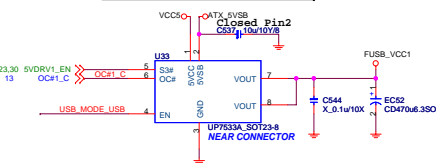
### USB POWER FOR PORT 0,1



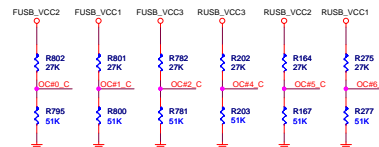
### USB POWER FOR PORT 4,5



### USB POWER REAL PORT 2,3

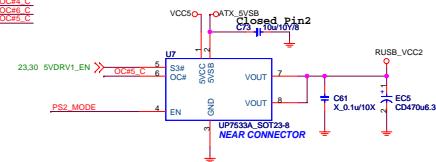


USB\_MODE for USB voltage  
H:Follow 5VSB  
L:Always off

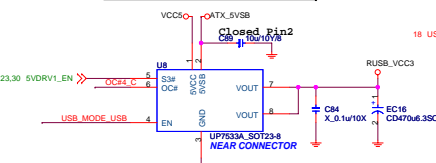


## Front USB Connector

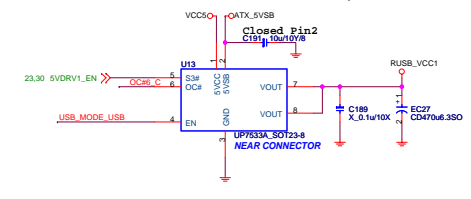
### USB POWER FOR PORT 10,11



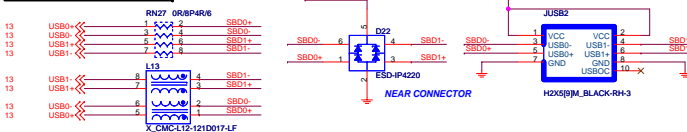
### USB POWER FOR PORT 8,9



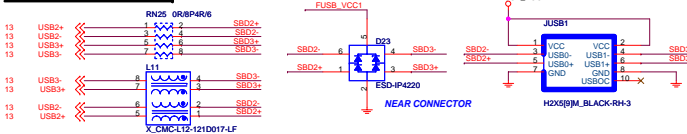
## USB POWER FOR PORT 12,13



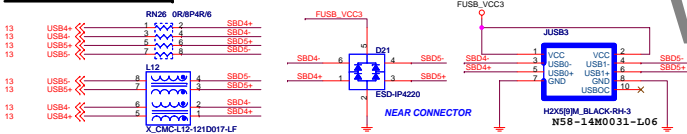
### FRONT USB PORT 0,1



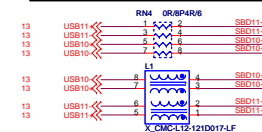
### FRONT USB PORT 2,3



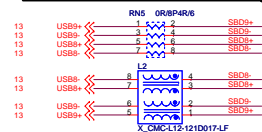
### Front USB PORT 4,5



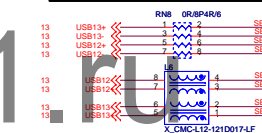
### REAR USB PORT 10,11



### REAR USB PORT 8,9

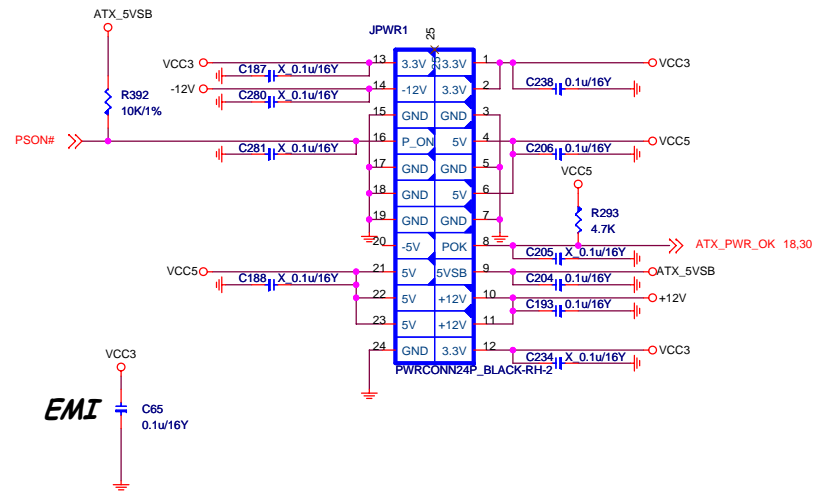


### REAR USB PORT 12,13

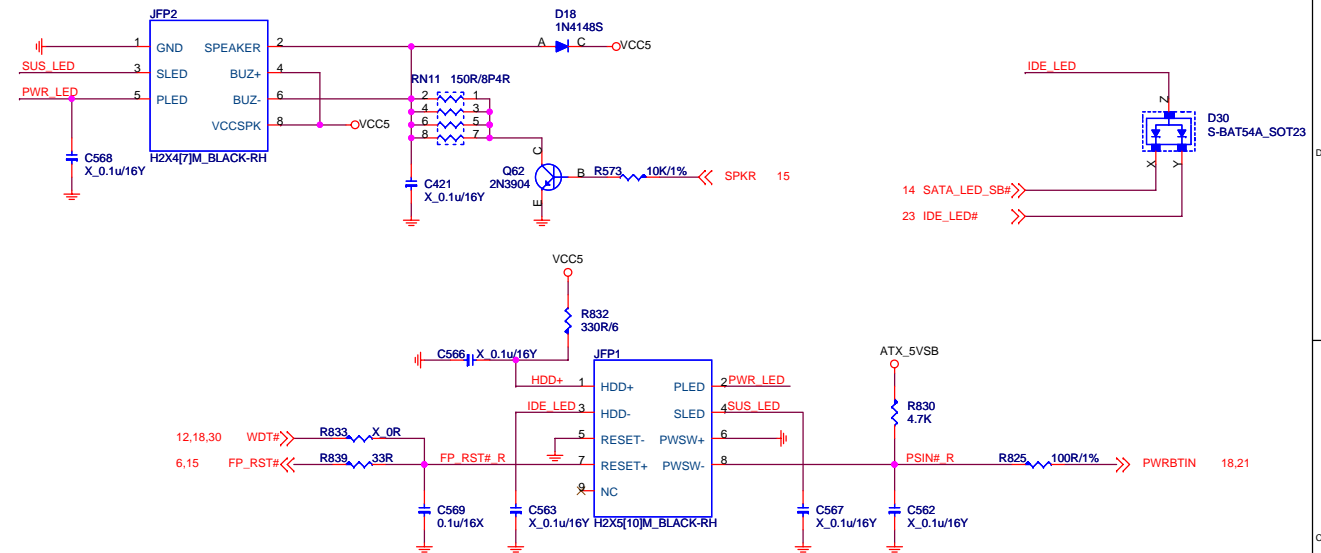


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## ATX POWER CONNECTOR



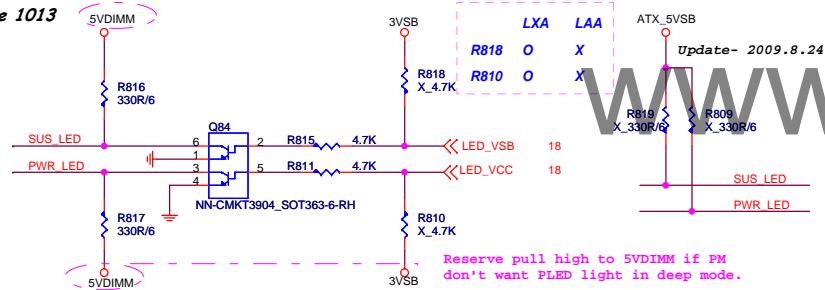
## FRONT PANNEL



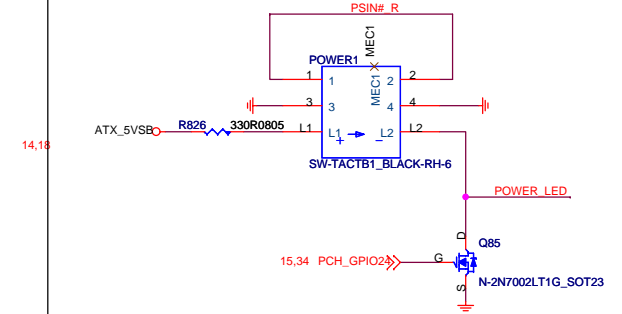
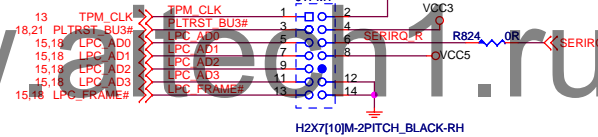
## LED ( for Fintek 71889)

If use F71889ED LED Ctrl,  
SIO LED\_VCC / LED\_VSB can not to use.

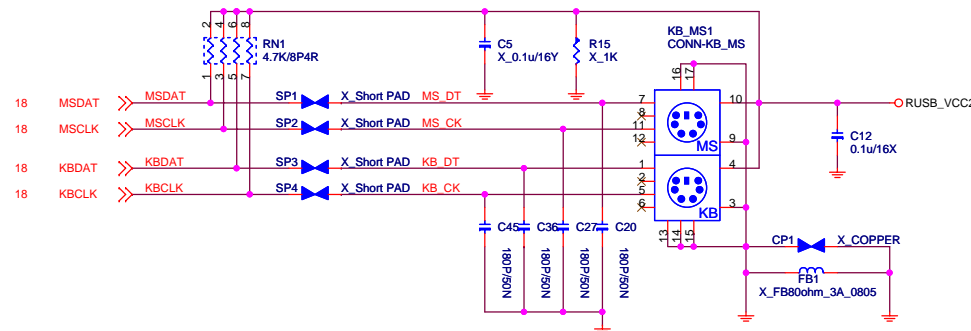
Update 1013



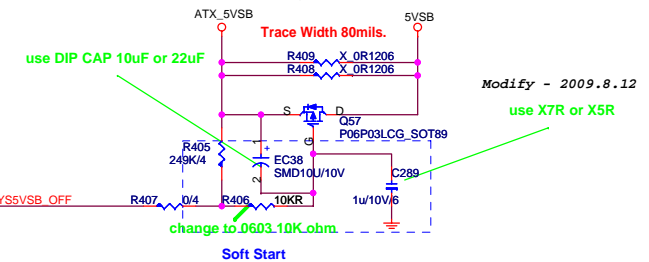
## TPM



## PS2 KEYBOARD & MOUSE CONNECTOR



## 5VSB Power Switch



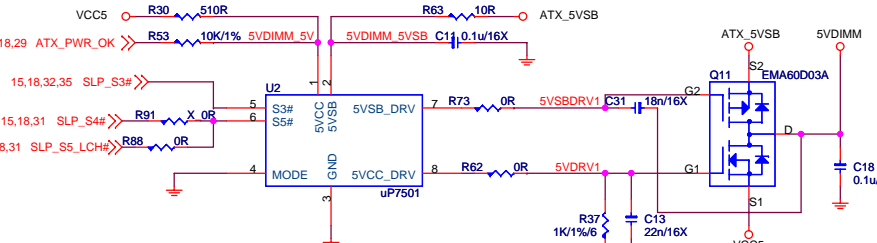
MICRO-STAR INT'L CO.,LTD

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5VDIMM FOR DDR

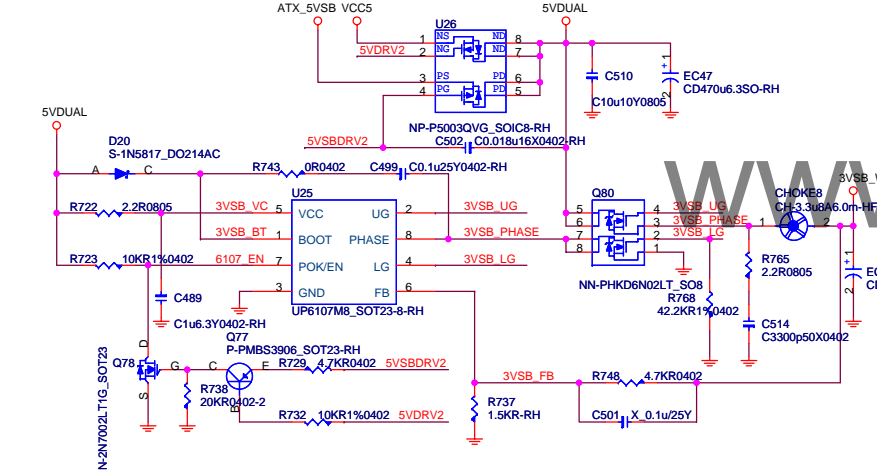


If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#, else use SLP\_S4#.  
R88 stuff, R91 remove

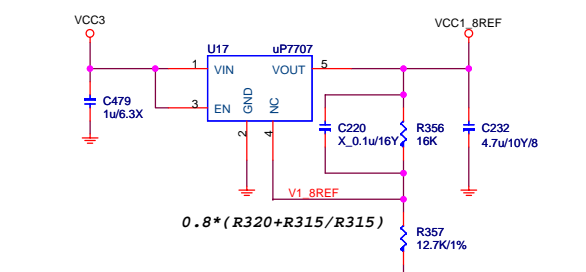
Used SLP\_S5# for AMT

7501 Mode  
H:Support S0/S3/S5  
L:Support S0/S3

Deep Mode WOL LAN Power CTRL Circuit

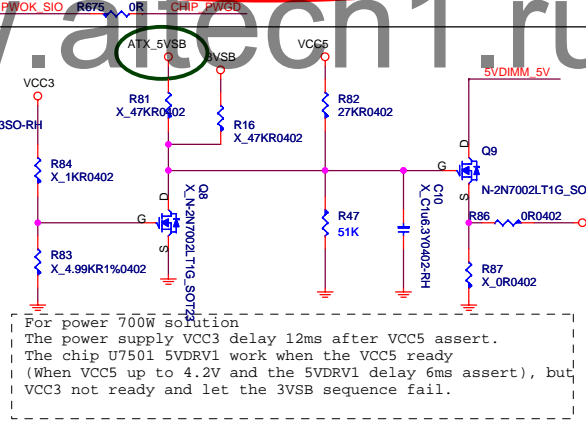
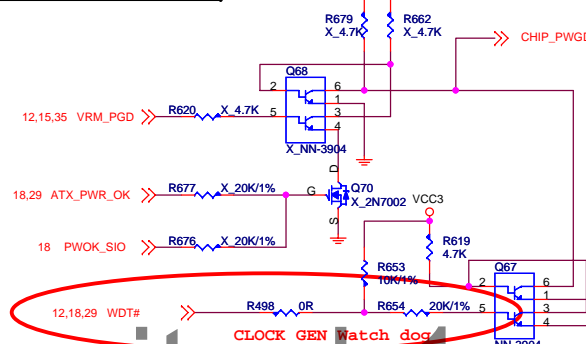


VCC1\_8REF



PWROK\_DELAY

VID before PWROK >3ms

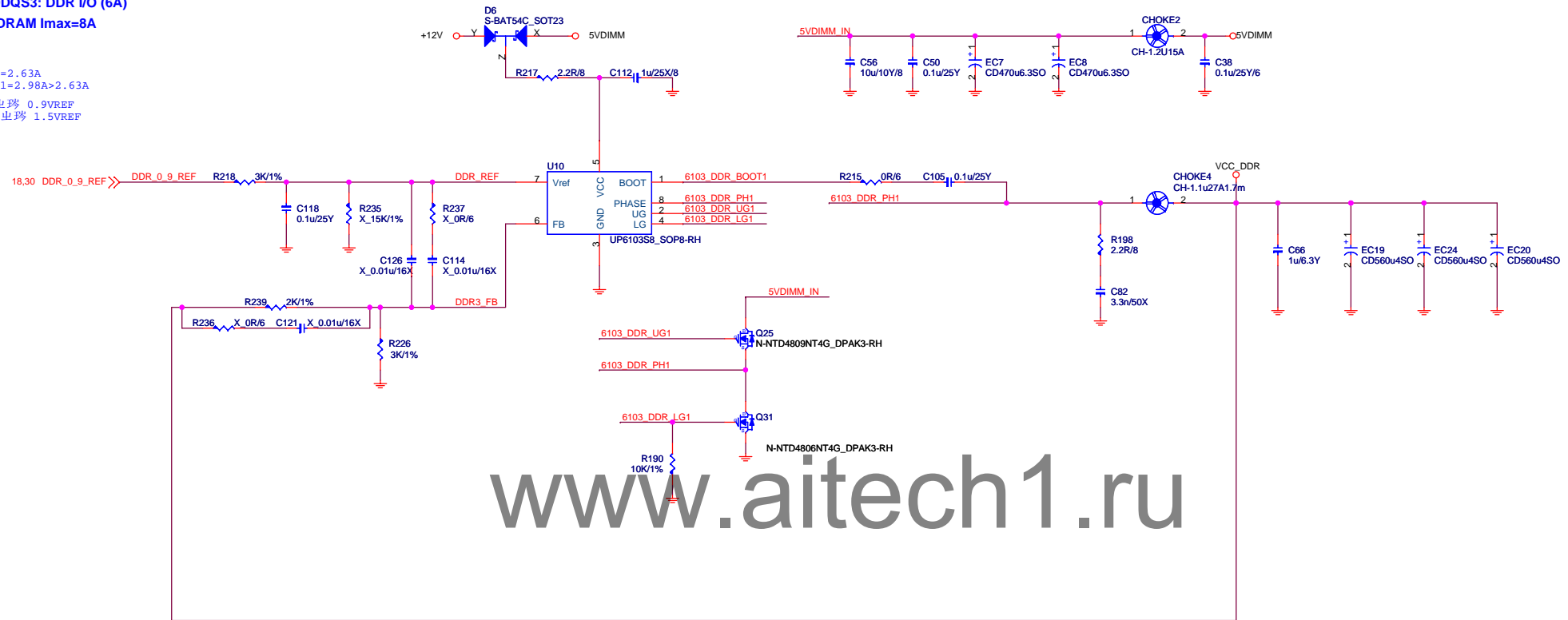


DDR3\_1.5V

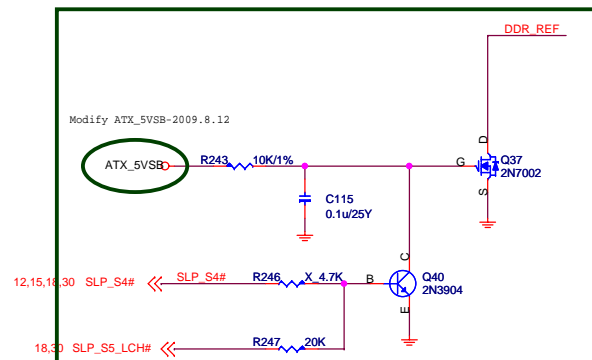
$$21.25A=6A+8A+0.75A+6.5A$$

V1.5DDQS3: DDR I/O (6A)  
DDR DRAM I<sub>max</sub>=8A

Tripple=2.63A  
1.49\*2\*1=2.98A>2.63A  
SIO 业界 0.9VREF  
6264 业界 1.5VREF



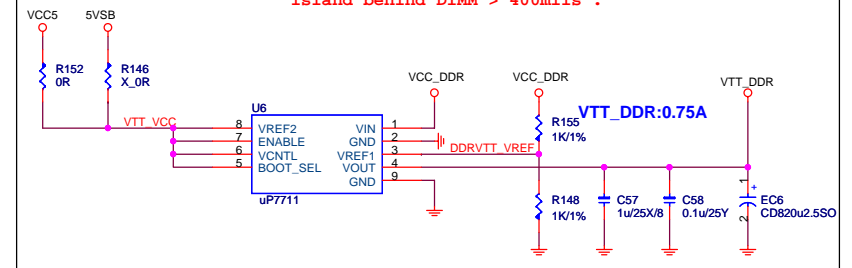
If you use LAA and can support deep\_s3,  
please use SLP\_S5\_LCH#, else use SLP\_S4#.  
R247 stuff, R246 remove



Only for meet Intel power down sequence.

### DDR VTT Power

To CPU Copper trace width > 250mils , Fill  
island behind DIMM > 400mils .



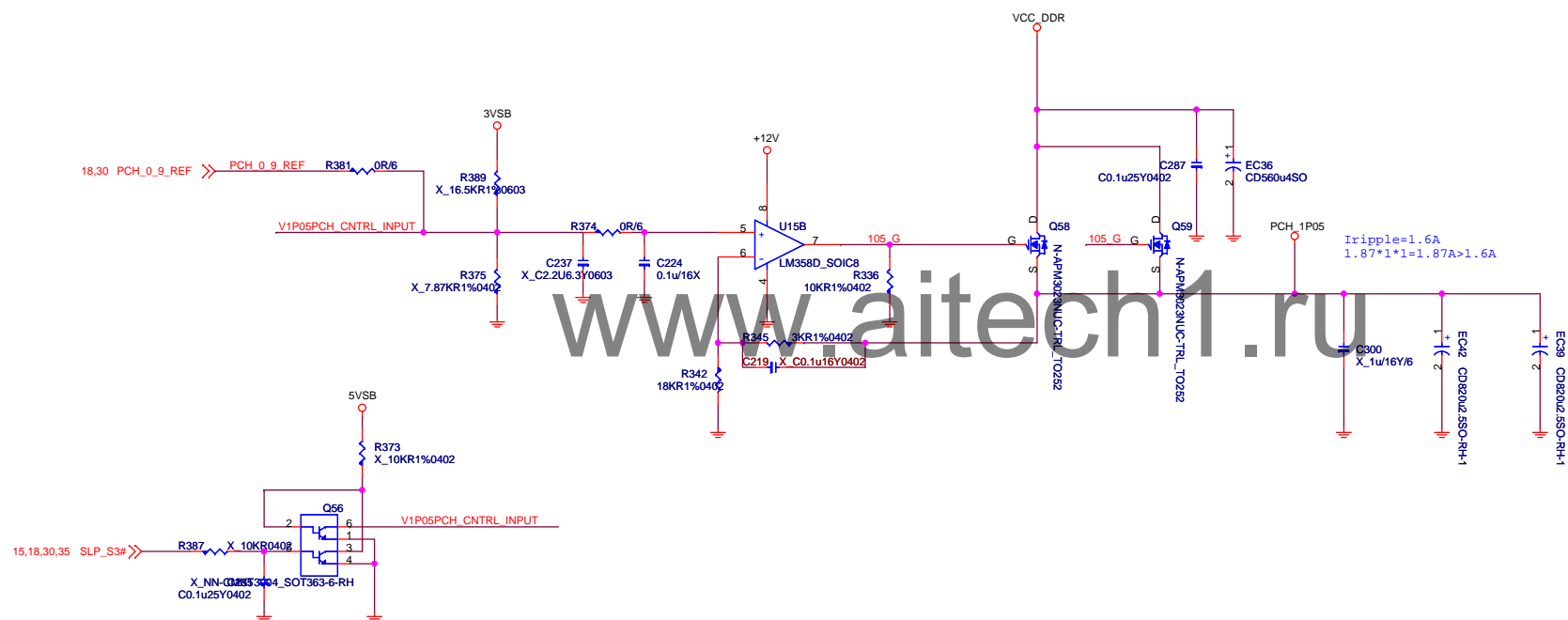
MICRO-STAR INT'L CO.,LTD

MS-7638

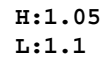
Size	Document Description	Rev
Custom	DDR POWER - UPI6103_1-Phase	10
Date: Monday, January 18, 2010	Sheet 31	of 38

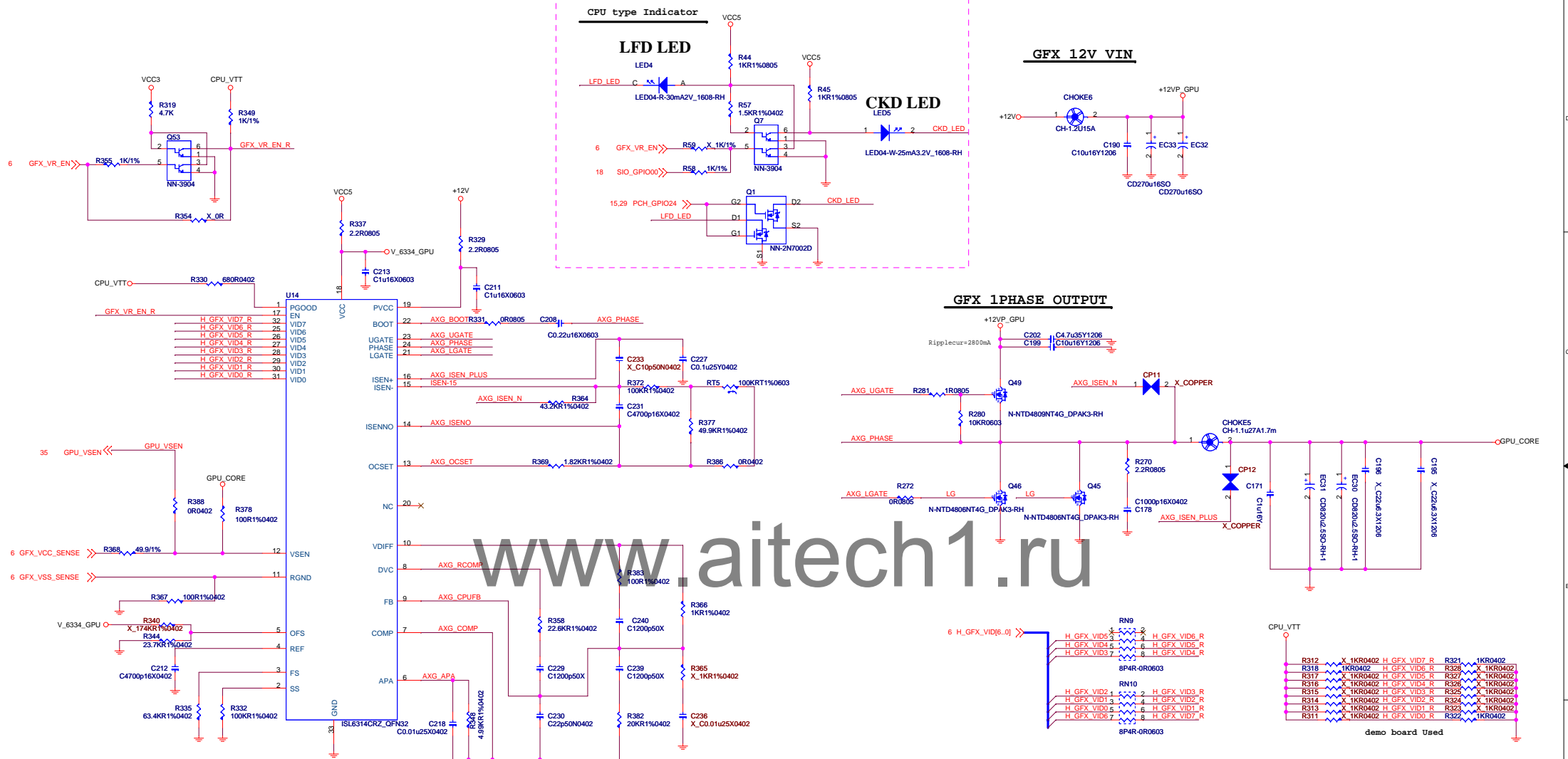
# PCH Core 6.8A

V1.05PCHS0: Vcc, VccExp, VccDMI, VccSATA,  
VccSATAPLL, VccAUPLL, VccSSC, VccDIFFCLK,  
VccDIFFCLKN, VccUSBCORE, VccDPLL, VccDPLL\_EXP, VccDPLL\_FDI (4.5A)  
V1.05MEM: VccMEW, VccAUX, VccME (2.3A)




**VTT50: 1.1V/1.05V CPU Uncore, MCP I/O (30A)**  
 $I_{ripple}=8.28A$   
 $6.1*2*1=12.2A>8.28A$

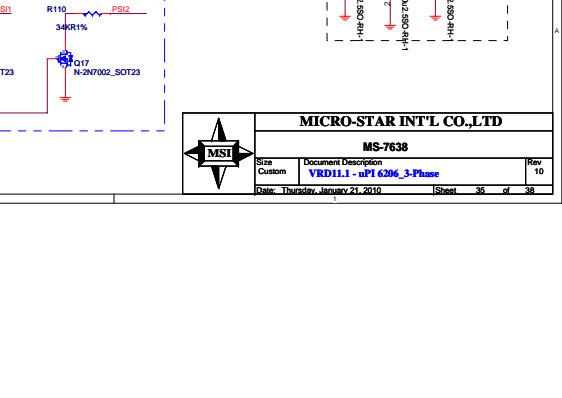
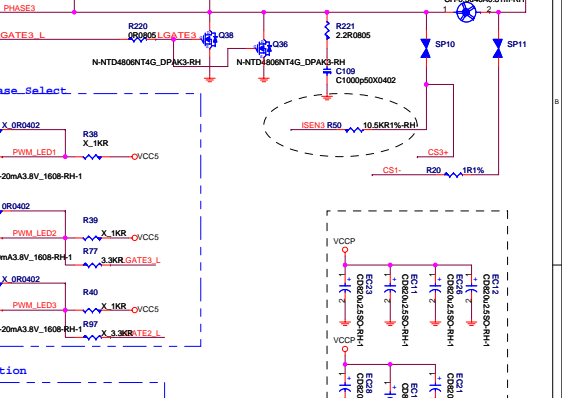
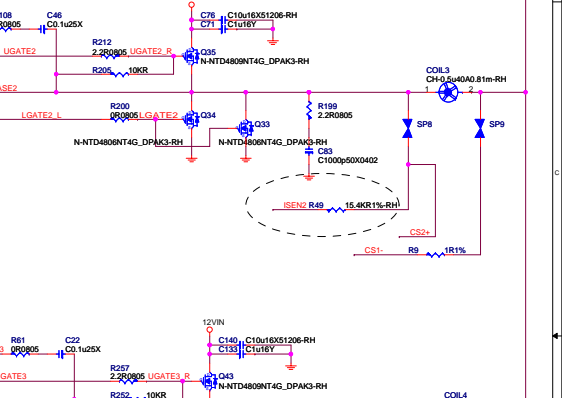
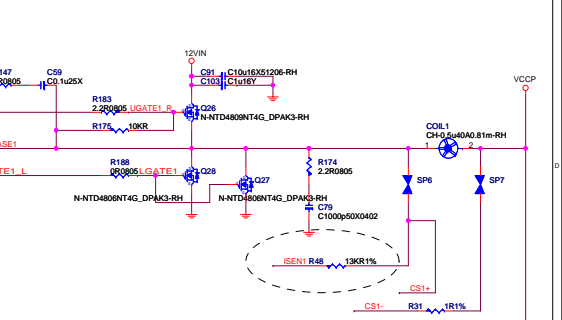
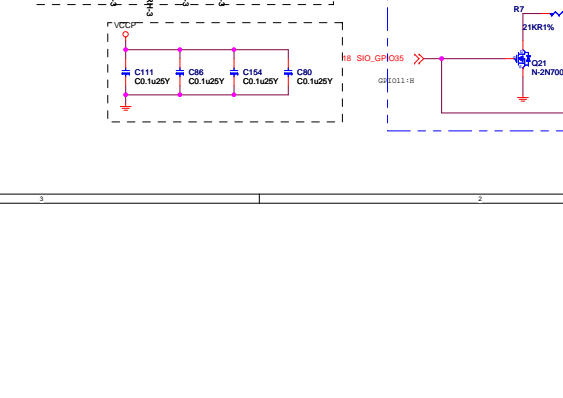
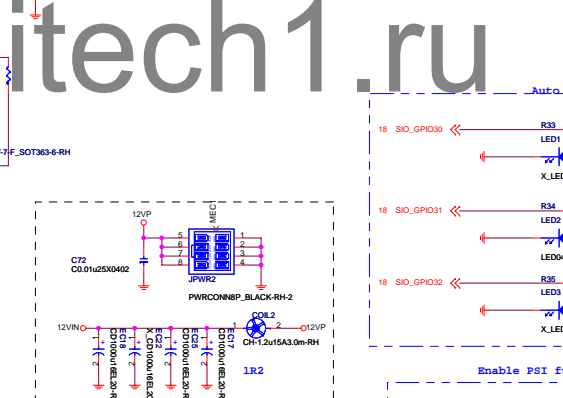
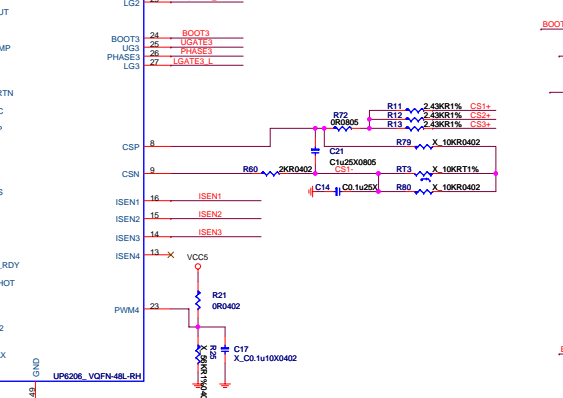
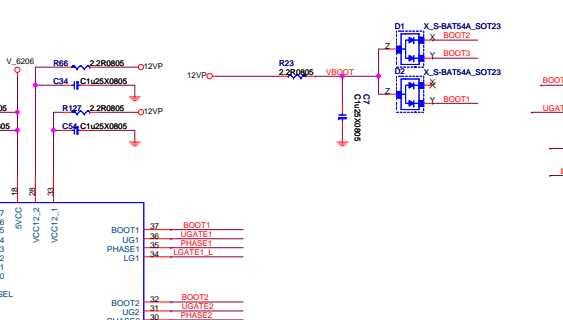
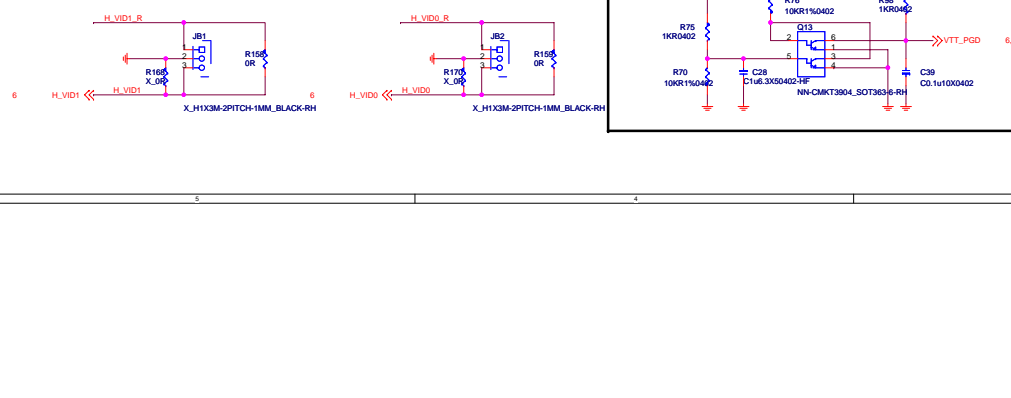
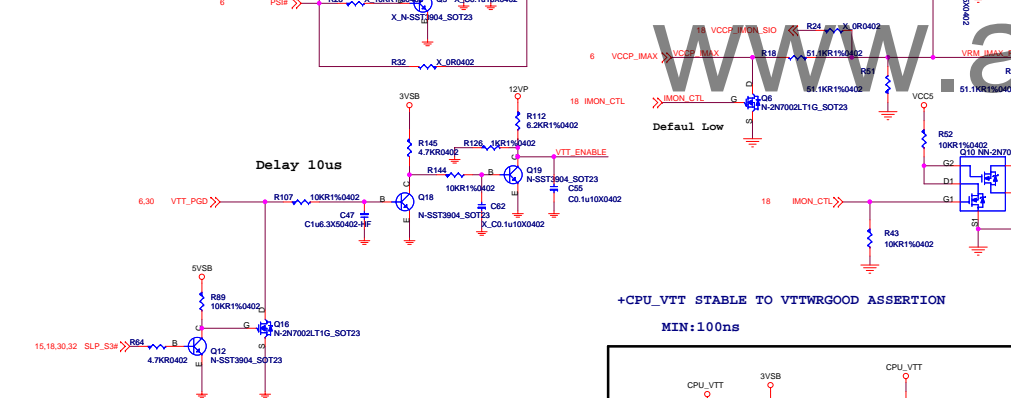
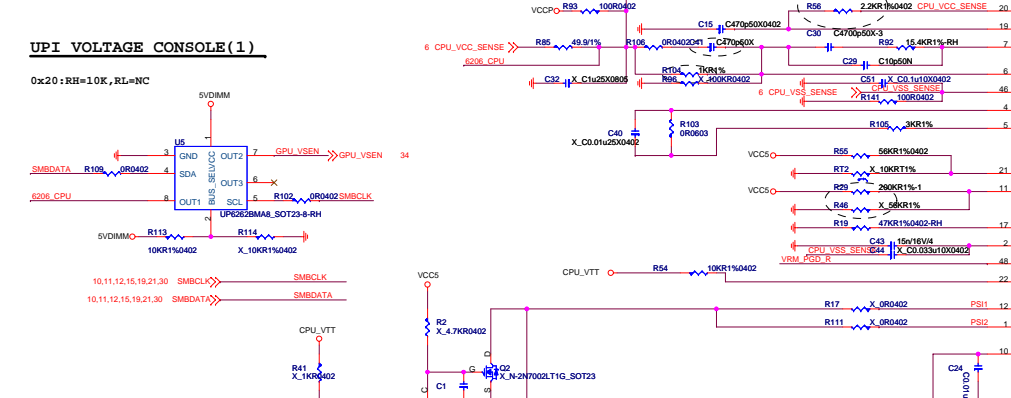
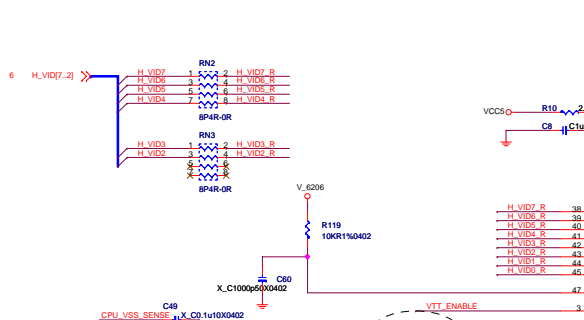
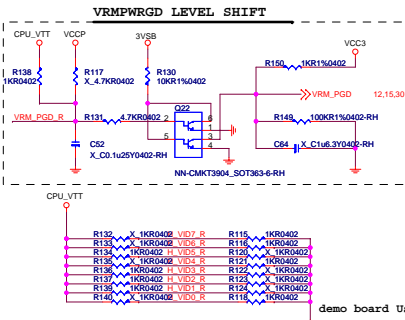




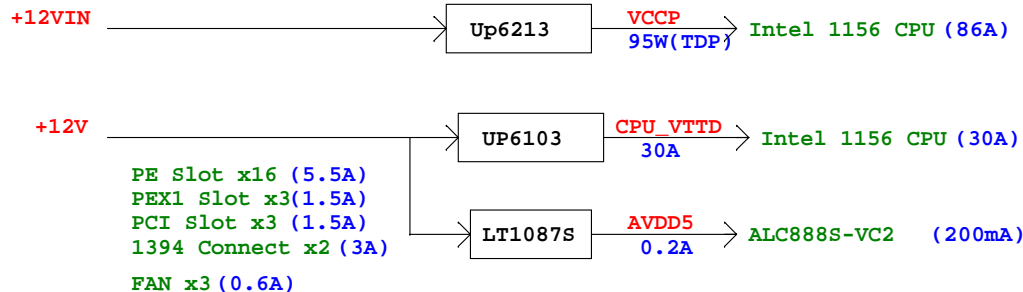
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GFX VR (Clarkdale Only)  
Switcher (7 VID), 16A TDC, 25A Imax

		MICRO-STAR INT'L CO.,LTD	
		MS-7638	
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		GPU PowerISL6117_1-Phase	10
Date: Monday, January 11, 2010		Sheet 34 of 38	

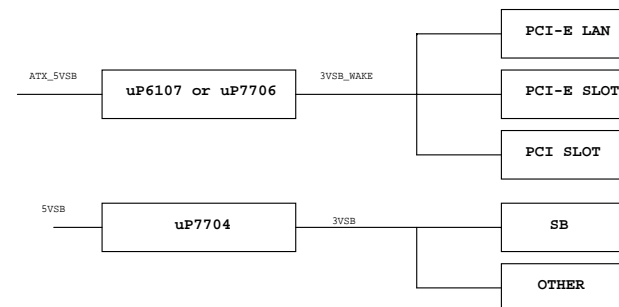


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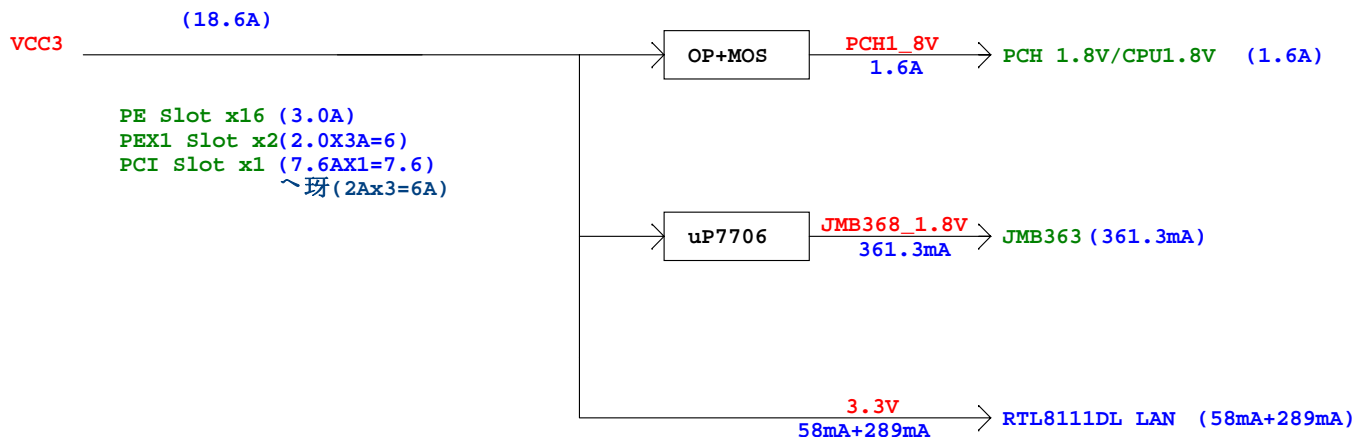
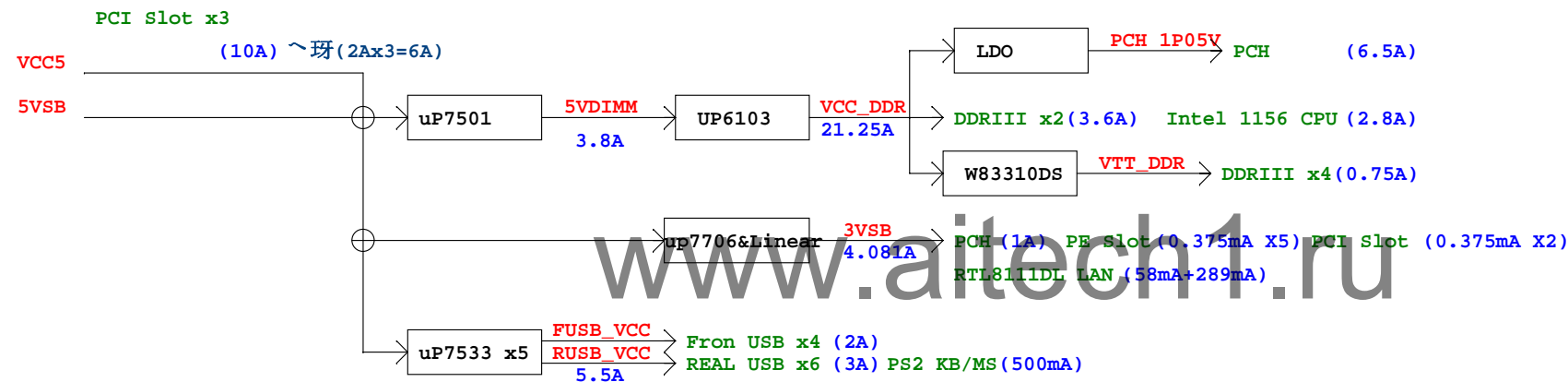


## 3VSB and 3VSB\_WAKE POWER MAP

Add- 2009.9.28



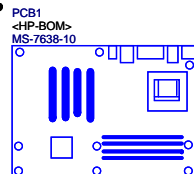
## Power Delivery



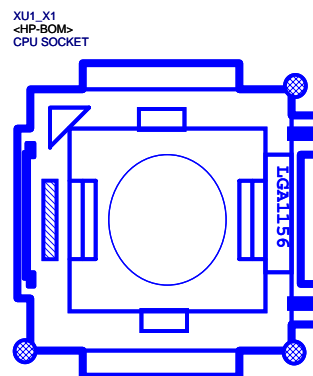
MICRO-STAR INT'L CO.,LTD			
MS-7638			
Size	Document Description		Rev
Custom	Power Map		10
Date: Monday, January 11, 2010		Sheet 37 of 38	



## PCB

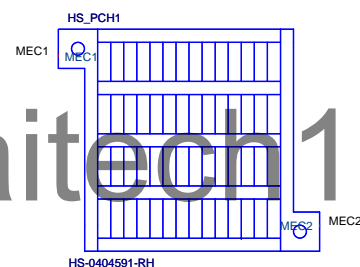


## CPU SOCKET

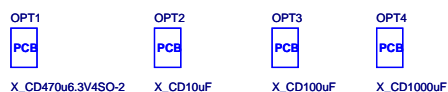


## HEATPIPE

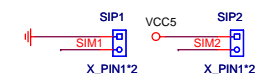
## BATTERY



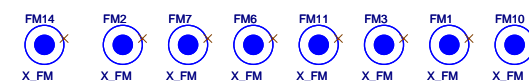
## EL CAP



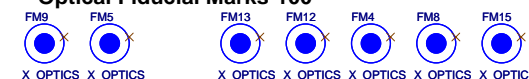
## Simulation



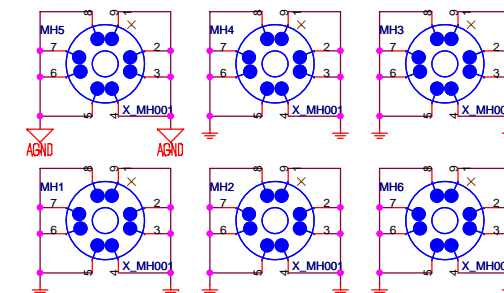
## Optical Fiducial Marks-120



## Optical Fiducial Marks-100



## Mounting Holes



H55EB3:3孔audio (888S VC2) ,GB LAN, OC-switch 不上, DVI,HDMI 不上,  
JMB368 不上(IDE 也不上), APS LED 不上 (SW APS) 半固.  
H55SG6DVI:Full spec